DESIGN AND ANALYSIS OF CERAMIC-TSOP PACKAGE APPROVED

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ABSTRACT

This research describes a novel ceramic thin-small-outline package (C-TSOP) to meet the thermal performance and long-term reliability considerations of today's low-pin-counts and high-performance electronic devices, especially for memory devices. To improve the disadvantages of molding compound and to simplify fabrication process, molding compound is replaced by ceramic-like stiffener which is adhered to the leadframe by a tape or adhesive as shown in Figs. 1(a) and 1(b). The ceramic-like stiffener would overcome the low thermal conductivity problem of molding compound in a conventional LOC-TSOP (Fig. 2) and increase the efficiency of thermal dissipation of the LOC-TSOP. In this research, three-dimensional (3D) nonlinear finite element models of both the conventional and novel LOC-TSOP have been established. Various heat generations are applied to the 3D nonlinear models under a natural convection condition for evaluating heat dissipation capability and thermal resistance of the packages. Moreover, the material properties and solder joints reliability of the packages are also investigated. In order to compare the solder joints reliability of the novel LOC-TSOP to the conventional LOC-TSOP, a nonlinear finite element method is used to analyze the physical behaviors of packages under a thermal loading condition. The results are compared with the experiments reported in the literatures in order to demonstrate the accuracy of the finite element models. From the results, it can be concluded that the novel C-TSOP package implies excellent thermal performance and appropriate solder joint reliability.

INTRODUCTION

The Lead-on-Chip Thin-Small-Outline Package (LOC-TSOP) is a general packaging technique in present low-pin-counts, high-speed memory devices. The photograph of the conventional LOC-TSOP assembly is shown in Fig. 2. The LOC-TSOP has a high chip/package dimension ratio, relative fine pitch and light weight over the leaded packages. Because of these advantages, LOC-TSOP is used widely in memory devices. However, as the requirement of power dissipation and high density of memory devices continuously increase, the thermal performance of conventional TSOP may not meet the demands. Accordingly, a novel C-TSOP has been introduced in this research. Thermal performance and solder joint reliability are two of the major issues of electronic packages. There are several factors influencing thermal performance and reliability significantly, including the structure and geometry of the assembly, dimensions of the components and material properties. For reliability, molding compound plays a very important role in preventing the entire package from damage and enhancing the strength of the conventional TSOP. On the other hand, molding compound presents lower thermal conductivity, resulting in poor thermal dissipation of the LOC-TSOP. Several investigators have attempted to enhance the thermal performance of leaded packages by using a copper leadframe or heat spreader. Aghazadeh et al. (1990) improved the thermal resistance by the application of a multilayer leadframe structure. Lai et al. (1999) used different shape die pads as heat spreaders for enhancing thermal dissipation. Cho et al. (2000) stacked TSOPs for high density memory devices. It performed good thermal performance because one of the chips could serve as a heat sink when the others are working. Although the copper leadframe and the heat spreader have good conductivity to enhance thermal performance, stress and strain problems, such as thermal expansion mismatch would be induced.

The thermal stress due to environmental temperature change is another important consideration of electronic packages. Compare with other leaded packages, LOC-TSOP has poor thermal fatigue resistance. Lau et al.

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(1992) investigated the solder joint reliability of TSOP under thermal loading. Mei (1996) predicted the thermal fatigue life of the TSOP solder joint using accelerated thermal cycling. These investigators indicated that the TSOP type packages have large local thermal expansion mismatch between silicon chips and molding compound, and global thermal expansion mismatch between packages and PC boards. The thermal expansion mismatch would cause large stress and strain that lead to failure at the solder joints during thermal cyclic load. Moreover, moisture and popcorn problems during fabrication also could significantly effect the reliability of packages. Ko et al. (1999) studied the warpage of LOC-TSOP. It indicated that the post mold curing on the package causes warpage and volume shrinkage of the package. The warpage effects would cause interconnect problems between packages and PC boards.

Since the CTE mismatch induced large stress and strain of the packages, the residual stress after packaging process would be a problem of LOC-TSOP. Most of the residual stress on the solder joint would be released during post baking. However, the volume shrinkage of the molding compound and adhesive would cause large residual stress. The volume shrinkage induced residual stress of the C-TSOP is lower than typical 54-lead TSOP, since there is no molding compound in the C-TSOP. Lau et al. (1992) set the TSOP package stress free at 25^0C without residual stress, the simulation results of the stress and strain behavior are matched with the experimental results. Therefore, the residual stress influence would not be included in this research.

This study uses a numerical method to simulate thermal resistance and solder joint elasto-plastic behaviors, and to predict thermal fatigue reliability. A 3-D nonlinear FEM model is applied to evaluate the junction temperature and temperature distribution of packages under natural convection condition. Furthermore, based on the calculated effective plastic strain and Coffin-Manson's law, the thermal fatigue life is also investigated. To demonstrate the accuracy of predictions, the simulated thermal fatigue life and thermal resistance were compared with the experiments available in the literature.

PACKAGE CONCEPT

Figure 1(a) illustrates the cross-sectional view of C-TSOP. Ceramic-like stiffeners and IC chips are adhered to a leadframe by adhesive or tape and the leadframe can be bonded to the electrodes on the chip. The bottom side of the package is the chip supporter that is adhered to the other side of the leadframe. The supporter consists of the same material as the ceramic-like stiffeners for enhancing the strength and the heat dissipation of the package. As shown in Fig. 1(b), the shape of the ceramic-like stiffeners is a loop around the silicon chip, and the top surface of silicon chip is exposed to the air. Compared to the conventional TSOP, the C-TSOP is manufactured without molding and curing process. It implies that the fabrication of the C-TSOP is a low temperature process and the volume shrinkage and warpage could be avoided. Moreover, it is very convenient to mount heat sink on the top surface of the package for high power dissipation packages. The novel packaging concept of C-TSOP is a pending patent.

FUNDAMENTAL THEORY

Thermal Resistance

Thermal resistance is commonly used as an index of thermal performance of electronic packages. Thermal resistance, R_{ja} is generally defined as:

$$R_{ja} = \frac{(T_j - T_a)}{P} \tag{1}$$

where T_j is the junction temperature, T_a is the ambient temperature and P is the dissipation power.

When the surface temperature is above the ambient temperature, a portion of heat is dissipated by convection. The heat transfer coefficient, h_c in a natural convection condition for small devices was suggested by Ellison and can be expressed as:

$$h_c = 0.83 f \left(\frac{\Delta T}{L_{ch}} \right)^n \tag{2}$$

where ΔT is temperature difference between the surface of the package and the ambient and L_{ch} is the characteristic length. The constants n and f were suggested by Ellison can be given as 0.33 and 1.0, respectively, for a horizontal plate facing upward and 0.33 and 0.5, respectively, for a horizontal plate facing downward.

The characteristic length L_{ch} can be defined as:

$$L_{ch} = \frac{WL}{2(W+L)} \tag{3}$$

where L is the length of the plate and W is the width of the plate.

Thermal Fatigue Life

When subjected to temperature cyclic loading, the solder joints would suffer from large strain/stress and cause major fracture mechanisms for the package. Therefore, thermal fatigue life is an important consideration of solder joint reliability. However, thermal fatigue test of electronic devices under thermal condition would take long computational time, thus, solder joints are tested numerically under accelerating thermal cycles in this study. The most common method to predict thermal fatigue life of the solder joints is the modified Coffin-Manson type relationship:

$$N_f = \theta (\Delta \varepsilon_{eq}^{pl})^{\eta} \tag{4}$$

where N_f is the number of cycles to failure and $\Delta\varepsilon_{eq}^{pl}$ is the incremental equivalent plastic strain.

For eutectic solder, the average values of η and θ at –50^{0}C, 35^{0}C and 125^{0}C determined by Solomon are -1.96 and 1.2928, respectively.

The incremental equivalent plastic strain is defined as:

$$\Delta\varepsilon_{eq}^{pl} = \frac{\sqrt{2}}{3}\sqrt{(\Delta\varepsilon_x^{pl}-\Delta\varepsilon_y^{pl})^2+(\Delta\varepsilon_y^{pl}-\Delta\varepsilon_z^{pl})^2+(\Delta\varepsilon_z^{pl}-\Delta\varepsilon_x^{pl})^2+\frac{3}{2}\Delta\gamma^{pl}} \quad (5)$$

where $\Delta\gamma^{pl} = \Delta\gamma_{xy}^{pl\ 2} + \Delta\gamma_{yz}^{pl\ 2} + \Delta\gamma_{zx}^{pl\ 2}$

$\Delta\varepsilon_x^{pl}$、$\Delta\varepsilon_y^{pl}$、$\Delta\varepsilon_z^{pl}$、$\Delta\gamma_{xy}^{pl}$、$\Delta\gamma_{yz}^{pl}$ and $\Delta\gamma_{xz}^{pl}$ are incremental plastic strain components acting on the solder joint. The accumulated equivalent plastic strain can be defined as:

$$\varepsilon_{eq}^{pl} = \sum \Delta\varepsilon_{eq}^{pl} \quad (6)$$

FEM MODELS

To simulate thermal performance and solder reliability of LOC-TSOP, three-dimensional nonlinear finite element (FE) models are established by using the commercial software ANSYS®. The finite element models were assumed steady state condition. Because of symmetry in geometry, one quarter model of the package is considered in this research. Figs. 3 and 4 show the 3-D finite element mesh model of a typical 54-lead TSOP and C-TSOP on PC board. The components of a typical LOC-TSOP in the FEM model are chip, leadframe, molding compound, solder and four-layer FR-4 PCB test board. The C-TSOP FEM model includes the following components, a chip, a leadframe, solder joints, adhesive, ceramic-like stiffeners and a PCB test board. The detailed material properties and dimensions of the package are listed in Tables I (Lau, 1991) and II, respectively. Because the accuracy of the finite element analysis result is highly dependent on the accuracy of material properties, the multi-linear and temperature-dependent material properties of solder, adhesive and molding compound are considered in this research. The temperature-dependent stress and strain curve of the solder and the adhesive are shown in Fig. 5 (Lau, 1991) and Fig. 6 (S. Liu et al., 1995), respectively. The temperature-dependent Young's modulus of the molding compound is shown in Table III (Lau 1991). The elasto-plastic nonlinear finite element models are based on kinematic hardening rule. To ensure convergence, the full Newton-Raphson method with a sub-step iteration is used.

In this study, thermal performance of the package is simulated based on the specification in JEDEC standards. An equivalent uniform heat source in the die ranging from 0.2W to 2W was employed in the FEM analysis. The ambient temperature and stress free temperature is at 25^{0}C. Thermal fatigue life of the solder joints was studied under an accelerating thermal cycling (ATC) test using FEM analysis. The temperature range varying from –40^{0}C to 125^{0}C as shown in Fig. 7 is applied in this analysis.

RESULTS AND DISCUSSION

Thermal Performance

Heat dissipation and thermal resistance of a C-TSOP and a typical 54-lead TSOP are predicted by 3-D nonlinear FEM analysis in this research. To study the thermal performance of the C-TSOP and the typical 54-lead TSOP, the dissipation power ranging from 0.2W to 2W under a natural convection condition are applied. Fig. 8 is the FEM result of temperature distribution of a typical 54-lead TSOP under 1W dissipation power. This figure shows the temperature decreases from the IC chip to the PCB. The major heat flow path of the package is from the chip, through leadframe to the PCB, and then into the air by convection. The maximum temperature is 91.78^{0}C and the corresponding thermal resistance of the package is 66.78(^{0}C /W). A similar temperature distribution of the C-TSOP under 1W dissipation power is shown in Fig. 9. The maximum temperature is 66.6^{0}C and the corresponding thermal resistance of the package is 41(^{0}C /W). The comparison of the junction temperature of a typical 54-lead TSOP and the C-TSOP is shown in Fig. 10. It shows that a higher dissipation power exhibits a higher junction temperature. The junction temperature of the C-TSOP is lower than that of the typical 54-lead TSOP. This is due to the ceramic-like stiffener that could dissipate heat more rapidly than the molding compound. It also indicates that when the maximum junction temperature of an electrical device is limited to 100^{0}C, the C-TSOP could bear 1.9W of power dissipation. However, the typical 54-lead TSOP could only bear 1.1W of power dissipation. This phenomenon is more significant at a higher dissipation power. It implies that the C-TSOP could accommodate a higher power dissipation in the future.

Figure 11 is the thermal resistance versus dissipation power predicted by FEM analysis. When the dissipation power increases from 0.2W to 2W, the thermal resistance of the typical 54-lead TSOP decreases from 80(^{0}C/W) to 61.65(^{0}C/W), and the thermal resistance of the C-TSOP decreases from 50(^{0}C/W) to 38.57(^{0}C/W). The thermal resistance of the C-TSOP is 38% lower than the typical 54-lead TSOP. It is clear that the heat dissipation of the C-TSOP is more effective. Cho et al. tested the 64M DRAM to measure the thermal resistance. It indicated that the thermal resistance of 54-lead TSOP package is 71.3(^{0}C/W) at the dissipation power 0.42W. The thermal resistance prediction of the typical 54-lead TSOP is 73(^{0}C/W) at the dissipation power 0.42W in this research. A Comparison of the thermal resistance predicted from FEM analysis with the experimental results of 54-lead TSOP shows that the results of FEM analysis are reliable.

Figures 12 and 13 show the temperature gradient of the typical 54-lead TSOP and the C-TSOP under 1W dissipation

power, respectively. The temperature gradient distribution of the C-TSOP is more uniform than the typical 54-lead TSOP at the leadframe. It indicates that the heat generated by the chip component within the C-TSOP could dissipate rapidly in the package. Table IV shows the comparison of the thermal resistance between different leadframe conductivity under dissipation power 1W of the typical 54-lead TSOP. Since the molding compound of the typical 54-lead TSOP only could dissipate less heat than the C-TSOP, major portion of heat has to be dissipated through conduction from the leadframe to the PCB. It is verified that the ceramic-like stiffener has a significant influence on heat dissipation of the package.

Solder Joint Reliability

The 3D-nonlinear finite element models are used to simulate the accelerated thermal cycling, temperature varying between -40^0C and 125^0C in this research. The average equivalent plastic strain of the typical 54-lead TSOP after one thermal cycle load is shown in Fig 14. It is seen that the high average equivalent plastic strain occurs at the edge of corners of the solder joint of the package, and decreases rapidly to a smaller value from the concentrated zone. The maximum plastic strain locates at the leadframe/solder interface inside the solder joint. The strain concentration zone would cause the crack initiation. It is noted that the crack propagation is the major failure mode of the package during thermal cyclic loading. The contour plot of the average equivalent plastic strain of the C-TSOP is shown in Fig. 15. These two types of TSOP have a similar thermal fatigue behavior. The maximum average equivalent plastic strain locates at the leadframe/solder interface inside the corners of the solder joint of the C-TSOP. The accumulated average equivalent plastic strain of the C-TSOP and the typical 54-lead TSOP by one thermal cycle load are shown in Fig. 16. The maximum average incremental equivalent plastic strain $\Delta\varepsilon_{eq}^{pl}$ of the typical 54-lead TSOP was 0.0082 in one cycle and that of the C-TSOP was 0.01027. Based on the modified Coffin Manson's relationship, the solder joint of the typical 54-lead TSOP has an average fatigue life of 15866 cycles and that of the C-TSOP is 10206 cycles. It is reasonable that the thermal fatigue life of the typical TSOP is higher than that of the C-TSOP because failure during thermal cycling is primarily caused by thermal expansion mismatch. The coefficient of thermal expansion (CTE) of the molding compound and the PCB is about 15ppm/^{0}C, however, the CTE of the ceramic-like stiffener of the C-TSOP is 7ppm/^{0}C. Consequently, the CTE mismatch between the C-TSOP and the PCB is larger than the typical 54-lead TSOP. The CTE mismatch would induce a large strain at the solder joint of the C-TSOP. Table V shows the safe thermal fatigue life suggested by Solomon, the thermal fatigue life of the typical 54-lead TSOP and the C-TSOP in this research. It is known that both of the thermal fatigue life of the packages pass the safe average thermal fatigue life of 7320 cycles, although the thermal fatigue life of the C-TSOP is lower than the typical 54-lead TSOP.

CONCLUSIONS

In order to study the thermal/mechanical characteristic of the novel C-TSOP, thermal performance and solder joint reliability of the C-TSOP and the conventional TSOP are simulated by the 3D nonlinear FEM analysis in this research. From the results of analysis, the following conclusions are made:

1. The junction temperature of the C-TSOP is lower than the typical 54-lead TSOP because the ceramic-like stiffener could dissipate heat more rapidly than the molding compound.
2. The thermal resistance of the C-TSOP is lower than the typical 54-lead TSOP by about 38%.
3. Both the typical 54-lead TSOP and the C-TSOP have the maximum average equivalent plastic strain located at the leadframe/solder interface inside the corners of the solder joint.
4. Both the thermal fatigue life of the packages pass the safe average thermal fatigue life cycles.
5. The novel C-TSOP package has excellent thermal performance capability and appropriate reliability.

ACKNOWLEDGMENTS

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Table I Material properties of the FEM models

	Chip	Lead-frame(Alloy 42)	Molding compound	Adhesive	60Sn/40Pb Solder	PCB	Ceramic like stiffener
Thermal conductivity (W/m.K)	148	15	0.708	1.6	50	Kxx=17 Kyy=17 Kzz=0.3	21
Young's module (GPa)	112.4	148	temperature dependent	temperature dependent	temperature dependent	11	350
Poisson	0.28	0.3	0.3	0.25	0.35	0.28	0.3
CTE (ppm/^{0}C)	2.62	5	15	$<0^0$C = 90 $>0^0$C =160	25	15	7

CTE: coefficient of thermal expansion

Table II Dimensions of the packages

Package size	21.7×10.2×1 mm
Die size	11.2×5.6×0.325 mm
PCB size	101.6×114.3×1.57 mm
Leadframe thickness	0.150 mm

Table III Temperature-dependent Young's modulus of the molding compound

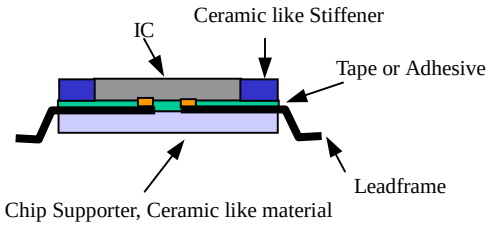
Temperature (K)	E (Gpa)
218	22.1
258	22.0
295	21.9
348	19.8
398	12.3

Table IV Thermal fatigue life of the packages

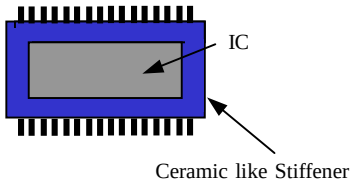
	Typical 54-lead TSOP	C-TSOP	Safe fatigue life
Thermal fatigue life (cycles)	15866	10206	7320

Table V Comparison of the thermal resistance between different leadframe conductivity of the typical 54-lead TSOP

Leadframe conductivity (W/m.K)	15	150
Thermal resistance (^{0}C/W)	66.78	33.89



(a) Cross sectional view of novel C-TSOP



(b) Top view of novel C-TSOP

Figure 1. Schematic illustrations of the C-TSOP: (a) Cross sectional view (b) Top view of the C-TSOP

Figure 2 Photograph of the conventional LOC-TOP (from Chipmos)

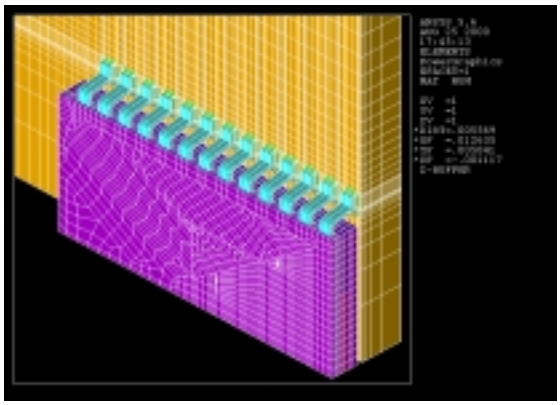


Figure 3. Finite element mesh model of the typical 54-lead TSOP on PC board

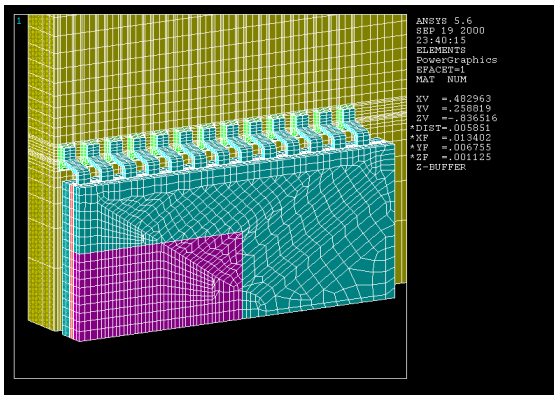


Figure 4. Finite element mesh model of the C-TSOP on PC board.

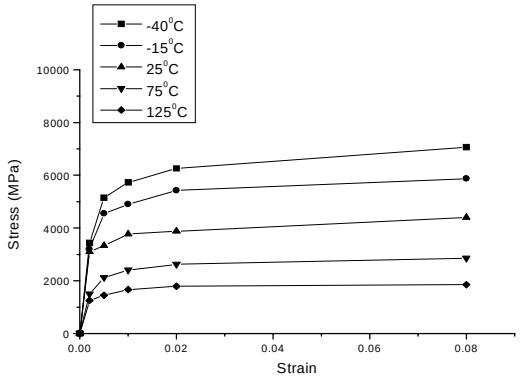


Figure 5. Temperature dependent stress and strain curves of the 60Pb/40Sn solder

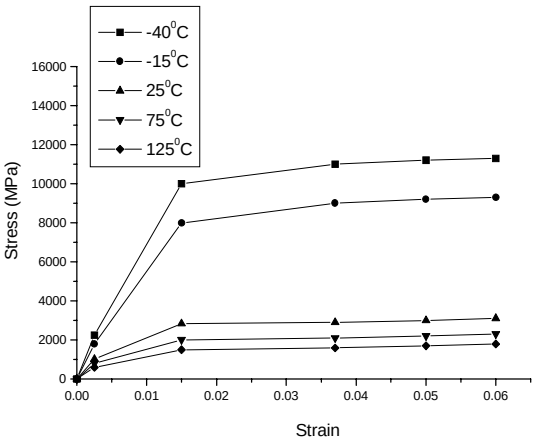


Figure 6. Temperature dependent stress and strain curves of he adhesive

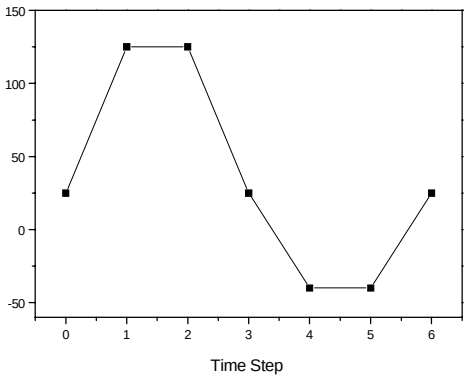


Figure 7. Thermal cyclic loading profile

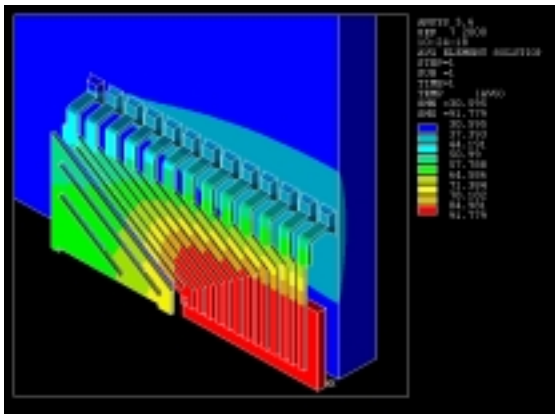


Figure 8. Temperature distribution of the typical 54-lead TSOP in natural convection condition

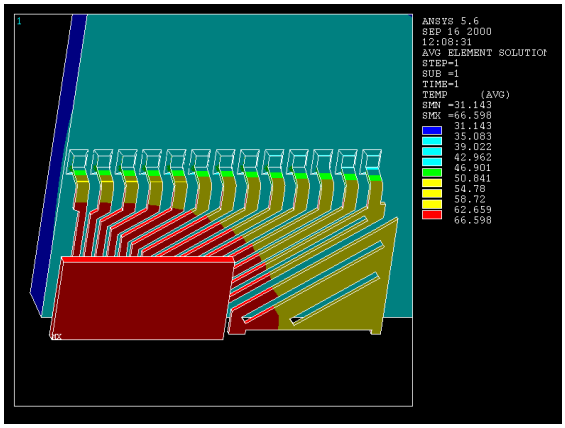


Figure 9. Temperature distribution of the C-TSOP in natural convection condition

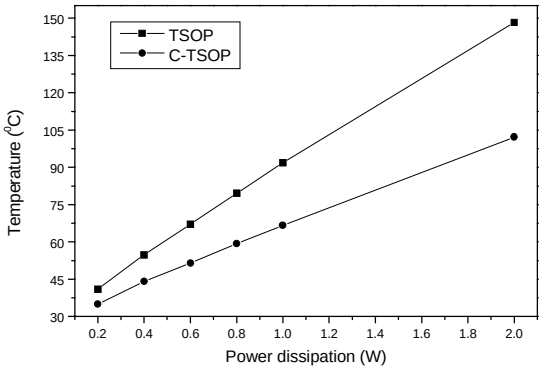


Figure 10. Junction temperature of the typical 54-lead TSOP and the C-TSOP in natural convection mode

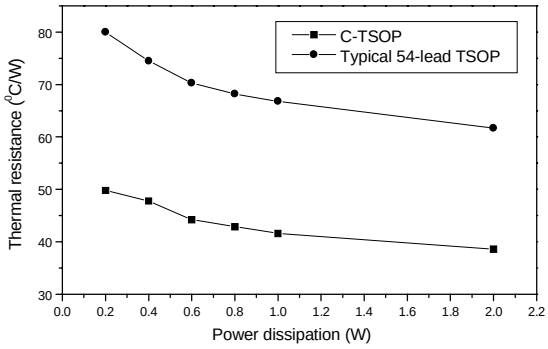


Figure 11. Thermal resistance of the typical 54-lead TSOP and the C-TSOP in natural convection mode

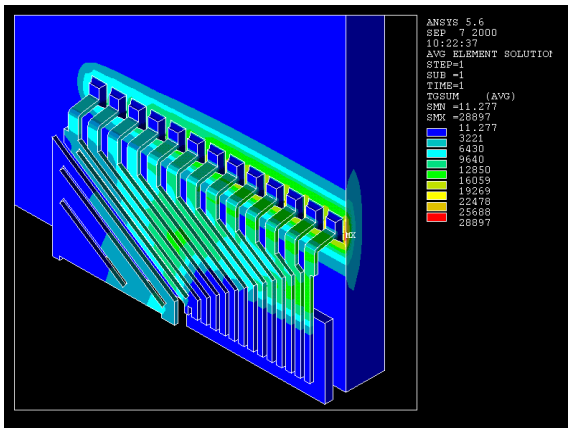


Figure 12. Temperature gradient of the typical 54-lead TSOP in natural convection condition

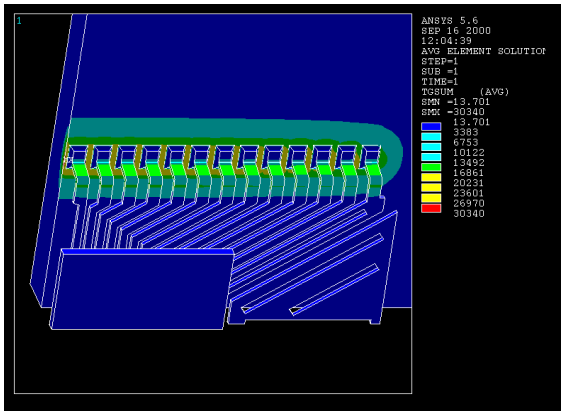


Figure 13 Temperature gradient of the C-TSOP in natural convection condition

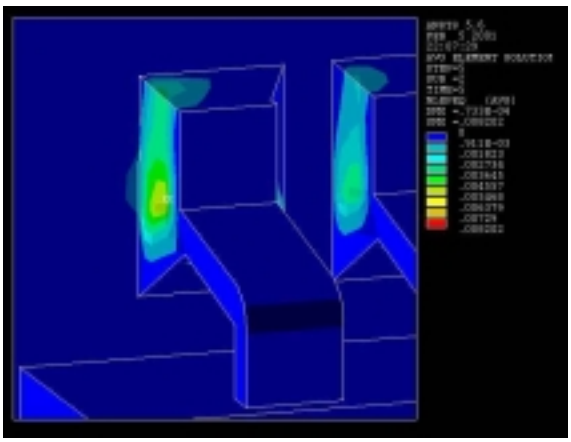


Figure 14. Average equivalent plastic strain of the typical 54-lead TSOP after one thermal cycle load

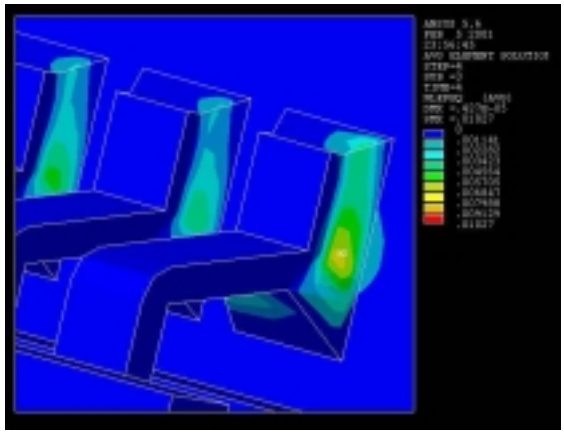


Figure 15. Average equivalent plastic strain of the C-TSOP after one thermal cycle load

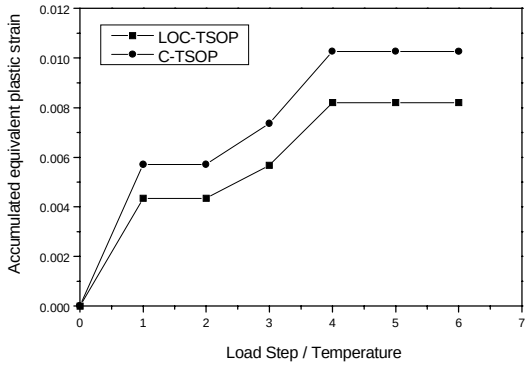


Figure 16. Accumulated average equivalent plastic strain of the C-TSOP and the typical 54-lead TSOP