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A NOVEL SILICON BASE PIEZORESISTIVE PRESSURE SENSOR USING FRONT SIDE ETCHING PROCESS

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Abstract

By applying the etching via technology, this study proposes a novel front-side etching fabrication process for a silicon based piezoresistive pressure sensor to replace the bulk conventional backside micro-machining. The distinguishing features of this novel structure are chip size reduction and fabrication costs degradation. In order to investigate the sensor performance and the sensor packaging effect of the structure proposed in this research, the finite element method was adopted for analyzing the sensor sensitivity and stability. The sensitivity and the stability of the novel sensor after packaging were studied by applying mechanical as well as thermal loading to the sensor. Furthermore, the fabrication process and the sensor performance of the novel pressure sensor were compared with the conventional back-side etching type pressure sensor for the feasibility validation of the novel sensor. The results showed that the novel pressure sensor provides better sensitivity than the conventional one, and the sensor output signal stability can

be enhanced by better packaging structure designs proposed in this study. Based on the above findings, this novel structure pressure sensor shows a high potential for membrane type micro-sensor application.

Keywords: Piezoresistive pressure sensor, Finite element method (FEM), Etching via, Front-side etching, Back-side etching

I. Introduction

Silicon base pressure sensors are one of the major applications of the piezoresistive sensor. Pfann [1] designed several types of semiconductor stress gauges to measure the longitudinal, transverse and shear stresses, as well as torque. A Wheastone bridge type gauge was employed for the mechanical signal measurement. The piezoresistance coefficient is a function of impurity concentration and temperature; hence the

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thermal effect will influence the measurement result of a piezoresistive sensor. Kanda [2] investgated a piezoresistance coefficient study about orientations, impurity concentration and temperature. Although the coefficient of piezoresistance π and the resistance R are temperature dependent, it can be compensated by an appropriate doping concentration of the resistors [2]. Lee [3] proposed another method to reduce the temperature coefficient of piezoresistor. In his study, ion-implanted trimming resistors were applied to compensate the temperature induced output voltage offset.

The package-induced stress and the thermal effect between different materials will influence the pressure sensor output linearity. Nysaether [4] measured the package-induced stress and the thermal zero shift of a packaged piezoresistive pressure sensor in the study. Recently, finite element analysis has been widely adopted for stress prediction, thermal effect reduction, packaging design and reliability enhancement of the piezoresistive sensor. Pancewicz [5] used FEM to obtain the output voltage of the pressure sensor, and he compared the simulation data with the experiment result. Nowadays, the measurement accuracy of silicon piezoresistive pressure sensor is more rigorous in many advanced applications. Therefore, the thermal and packaging effects should be taken into consideration for a better sensor accuracy. Schilling [6] applied FEM for sensor performance simulation, and discussed the packaging effects on silicon base piezoresistive pressure sensors. However, some design parameters such as packaging material and packaging structure that could influence the sensor stability were not discussed.

These days the silicon piezoresistive pressure sensor is considered a mature technology in the industry. Therefore, sensor fabrication costs become more significant in sensor design considerations. Several studies have investigated the pressure sensor in order to reduce the manufacturing cost and time. One of the solutions is using a thinner wafer. However, this solution becomes increasingly more difficult as the thickness of the wafer becomes thinner [7]. Another solution is to etch from the front side of the silicon wafer. Bryzek et al. [8] etched the silicon wafer from the front side and sealed it by using silicon fusion bonding. The resistors were ion implanted after wafer bonding and thinning. Although this front side etching process reduced the pressure sensor chip size, the manufacturing cost increased due to wafer bonding and wafer thinning.

For the above reasons, this study presents a novel fabrication process of a silicon base piezoresistive pressure sensor to reduce its mass production cost and to simplify its fabrication process. Furthermore, the packaging structure design is also considered to reduce the thermal as well as packaging effect of the pressure sensor.

II. Fundamental theory of piezoresistive pressure sensor

In this study, the mathematical relation between the piezoresistance and the output voltage of the pressure sensor will be introduced. Moreover, the introduced equations will be applied to finite element analysis.

For a membrane type piezoresistance pressure sensor, the

stress state on the resistors can be assumed to be plane stress $(\sigma_z = \sigma_{xz} = \sigma_{yz} = 0)$ condition and the shear stress $\sigma_{xy} <<$ the normal stress σ_x , σ_y . The most common situation of the piezoresistors under force loading is schematically in Fig. 1.



Fig. 1: The force/current situations that rules by (a) the longitudinal piezoresistance coefficient and (b) the transverse piezoresistance coefficient

In Fig. 1(a), considering a longitudinal force F_1 and a voltage V are applied on the piezoresistor. The uniaxial stress, electric field and current of this piezoresistor are all in the same direction (this direction not necessarily along a crystal axis). In Fig. 1(b), considering a transverse force F_t and a voltage V are applied on the piezoresistor. It could be found in fig. 1(b) that the uniaxial stress is in perpendicular to the direction of electric field and current. Therefore, two uniaxial stresses are defined: a longitudinal stress, σ_l and a transverse stress, σ_t for the membrane type piezoresistance sensor application. The relationship between resistivity variations and stress changes can be expressed as follows (Equation 1):

$$\frac{\Delta \rho}{\rho} = \pi_{l} \sigma_{l} + \pi_{l} \sigma_{l} \tag{1}$$

$$\pi_{1} = \pi_{11} + 2(\pi_{44} + \pi_{12} - \pi_{11})(l_{1}^{2}m_{1}^{2} + l_{1}^{2}n_{1}^{2} + m_{1}^{2}n_{1}^{2})$$
(2)

$$\pi_{t} = \pi_{12} - (\pi_{44} + \pi_{12} - \pi_{11})(l_{1}^{2}l_{2}^{2} + m_{1}^{2}m_{2}^{2} + n_{1}^{2}n_{2}^{2}) \quad (3)$$

Where 1 is the longitudinal piezoresistance coefficient and

t is the transverse piezoresistance coefficient. π_{ij} are the piezoresistance coefficients defined as a six by six matrix. For the cubic crystal structure of silicon, due to the symmetry conditions, the coefficients of matrix can reduce to three independent components: π_{11} , π_{12} , and π_{44} . I, m and n are the direction cosines between the <100> axis and a given crystal direction.

Figure 2 illustrates a membrane with four piezoresistors. If the resistors are correctly positioned on the membrane, the change in resistance of the first two piezoresistors will be opposite to that of the other two. Therefore the absolute value of the four-resistance variation can be equal. The resistors are connected in a Wheatstone bridge as shown in Fig. 2, where V_{in} is bridge-input voltage, and ΔV is the differential output voltage. The resistance change due to an unbalanced bridge can directly convert into a voltage signal under an applied pressure. For $\Delta R \ll R$, Equation (4) indicates the voltage and resistance relationship:

$$\Delta V = \frac{r}{(1+r)^2} \left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2} + \frac{\Delta R_3}{R_3} - \frac{\Delta R_4}{R_4} \right) V_{in}$$
(4)

Where $r = \frac{R_2}{R_1} = \frac{R_3}{R_4}$, ΔR_i is the i^{th} resistance change, R_i is the i^{th}

zero-stress resistance.

For $R = |R_1| = |R_2| = |R_3| = |R_4|$ in equation 4, the mechanical stress, the total resistance change (ΔR) and the output voltage relation, which neglect the dimensional changes, can be expressed as follows:

$$\frac{\Delta V}{V_{in}} = \frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} = \sigma_{1}\pi_{1} + \sigma_{t}\pi_{t}$$
(5)

The mechanical stresses obtained by FEM should be transferred into output voltage in such a way that the simulation stress value can be applied to predict the equivalent output electrical signal. Equation (6) indicates the output voltage, resistance and stress variation relation [10]:

$$\frac{\Delta V}{V_{in}} = \frac{\Delta R}{R} = \frac{\pi_l (\sum_{i=1}^n \sigma_{li} v_i) + \pi_i (\sum_{i=1}^n \sigma_{li} v_i)}{\sum_{i=1}^n v_i}$$
(6)

Where *i* is the piezoresistive element number of the finite element model, σ_{li} and σ_{ti} are the longitudinal and transverse stresses of the *i*th piezoresistive element, respectively, and v_i is the volume of the *i*th element on the piezoresistors. By applying this transfer method, the FEM simulation can be employed to predict the output voltage of the piezoresistive pressure sensor.



Fig. 2 Wheatstone bridge configuration of the four piezoresistors on the membrane

III. The Fabrication and The Packaging Process of the Novel Structure Pressure Sensor

This study proposes a novel process to fabricate a silicon base piezoresistive pressure sensor. The fabrication and the packaging processes comprise several steps, as shown in Figs 3(a) to 3(e). Since the detail fabrication process of the Wheastone-bridge and the piezoresistive units was described in the previous investigations [1,3,10]. This study focuses on the development of the silicon membrane fabrication by front side etching technology. The entire micromachining process steps can be accomplished at the front-side of the silicon substrate, due to the etching via technology being applied to form the silicon membrane. A P-type (100) silicon substrate with a N epi-layer and thermal oxide is employed in this study (shown in Fig. 3(a)). To fabricate the etching vias that penetrated the N epi-layer and the thermal oxide, the silicon wafer was etched by deep reactive ion etching (DRIE) (shown in Fig. 3(b)). Since the electrochemical etch-stop technique was adopted, the silicon wafer was immersed in the etching solution such as KOH. The etchant will be through the etching vias and in contact with the P-type substrate. The P-type substrate was etched anisotropically and the etching rate was highly depends on the silicon crystal orientation. Therefore, even though the shapes of the etching vias are circular, the eventual geometry of the silicon membrane will be squares (shown in Fig 3(c)). After the front side etching process, a silicon membrane with etching vias was fabricated. Figure 3(d) illustrates the top-view photograph of the etching vias. For pressure measurement, the etching vias were sealed by a high viscosity and photosensitive polymer, such as polyimide. After polymer coating, the sensor electrodes were opened for the signal output. Subsequently, the pressure sensor chip after wafer sawing was attached on the PCB board by an adhesive layer, and a wire bonding process is applied for the signal interconnection between silicon chip and PCB board. Finally, this packaged novel structure pressure sensor using etching via technology was established. Figure 3(e) indicates the 3/4 three-dimensional illustration of the packaged novel structure pressure sensor.

From the above fabrication and packaging processes, it can be observed that as comparing the fabrication and packaging processes with the conventional sensor, the novel pressure sensor needs two additional processes: DRIE and polyimide coating. However, the bonding or thinning process in the packaging process is avoided. Moreover, the etching via technology can accomplish a front-side etching process to replace the back-side etching process on the sensor fabrication. By employing the front-side etching process, the chip size can be reduced by at least 50% over the conventional method.





Fig. 3 Fabrication process flow of novel structure piezoresistive pressure sensor

IV. Finite Element Models

In order to study the sensor performance and the packaging effect of the novel structure pressure sensor, the finite element method was adopted to simulate the mechanical behaviors of the conventional pressure sensor and the novel structure pressure sensor. In this investigation, the commercial software ANSYS[®] was applied to analyze the mechanical behavior of the sensor under thermal and pressure loading.



Fig. 4 One-quarter finite element model of conventional piezoresistive pressure sensor

• The FEM model of the conventional pressure sensor

The quarter finite element models of the conventional pressure sensors were established in Fig. 4, since the packaged

pressure sensor device is has a quartered symmetry. The conventional pressure sensor finite element model comprised silicon chip, adhesive, glass and PCB substrate. The model contained 23,450 eight-node elements, and 79,614 D.O.F. The boundary conditions of the center surfaces were: x-directional displacement fixed on the y-z plane, y-directional displacement fixed on the x-z plane, and all nodes on the bottom side of PCB substrate fixed in x, y, and z directions. The ambient temperature and stress free temperature were assumed at 25° C.

• The FEM model of the novel structure pressure sensor

The quarter finite element models of the conventional pressure sensors were illustrated in Fig. 5. The novel structure pressure sensor comprised polyimide thin film, silicon chip, adhesive layer and PCB substrate. To study the performance of the novel sensor, there were three different models of the novel structure pressure sensor built: etching via diameter 10µm, 20µm and 30µm (shown in Fig. 8). On the other hand, to study the packaging and the thermal effect of the novel sensor, the FEM model with different adhesive layer thickness as well as different polyimide materials were established. The models contained 29,704 eight-node elements and 83,256 D.O.F. The boundary conditions of the novel structure pressure sensor are same as the conventional one. The ambient temperature and stress free temperature were assumed at 25°C. Table 2 lists the dimensions of PCB, glass, adhesive layer, silicon chip, silicon membrane and polyimide thin film. Table 3 indicates the material properties of PCB (FR-4), glass (7740), adhesive layer, silicon and polyimide.

Table 2. Dimensions of PCB, glass, adhesive layer, silicon chip and silicon membrane

	Length (µm)	Width (µm)	Thickness (µm)
PCB	10000	10000	1200
Glass	1800	1800	500
Adhesive (Conventional)	1800	1800	50
Adhesive (Novel 1)	1800	1800	50
Adhesive (Novel 2)	1800	1800	100
Silicon Chip	1800	1800	450
Silicon Membrane	600	600	20
Polyimide	1800	1800	5



Fig. 5 One-quarter finite element model of novel structure piezoresistive pressure sensor

	Young's Modulus	Poisson's Ratio	CTE (1/) (ppm)
	(Gpa)		
PCB (FR-4)	18	0.19	16
Glass (7740)	76	0.28	3.25
Adhesive	8.96	0.25	15
Silicon	112.4	0.28	2.62
Polyimide 1	3.49	0.34	30
Polyimide 2	3.49	0.34	20

Table 3. Material properties of pressure sensor

CTE: coefficient of thermal expansion

V. Finite Element Method Validation

In order to validate the finite element simulation results, an experiment of the conventional pressure sensor was employed. The piezoresistors with a Wheatstone-bridge configuration were located at (110) for the longitudinal direction and (110) for the transverse direction. Figure 6 shows the photograph of the packaged pressure sensor. The packaged pressure sensors were subjected to pressure and temperature loading. The loading condition was 10psi pressure loading with a temperature of -10° C to $+60^{\circ}$ C as the environmental condition, and the input voltage was 5 Volts.



Fig. 6 Top view of the packaged pressure sensor



Fig. 7 FEM simulation and experiment data comparison at 10psi pressure loading

The longitudinal coefficient π_l and transverse piezoresistance coefficient π_l was equal to $1/2(\pi_{1l}+\pi_{12}+\pi_{44})$ and $1/2(\pi_{1l}+\pi_{12}-\pi_{44})$, respectively. For low-doped p-type silicon and room temperature condition, the π_{1l} , π_{12} and π_{44} were 6.6x10⁻¹¹ (Pa⁻¹), -1.1x10⁻¹¹ (Pa⁻¹) and 138.1x10⁻¹¹ (Pa⁻¹), respectively [9]. The calculated longitudinal and transverse stresses were used to calculate the differential output voltage. Figure 7 presents the FEM simulation and experimental results. It was observed that

the FEM gave a good agreement with the experimental data. The average error between the FEM and the experiment was less than 3.5 % in this case. This experiment demonstrated that the FEM could predict the mechanical behavior and signal output of the silicon base piezoresistance pressure sensor.

VI. Results and Discussion

• Performance design of the novel structure pressure sensor

Since the fabrication process of the novel structure pressure sensor was developed, the sensor performance between the conventional and the novel pressure sensor should be studied to demonstrate the feasibility of the new design. In order to obtain the explicit relationship between the two structures, the FEM simulation was adopted to study the output voltage variation in this investigation.





Fig.8 The FEM model of the novel pressures ensor with etching via of (a)10 μ m, (b)20 μ m and (c)30 μ m

In order to investigate the output signal sensitivity of the novel pressure sensor, the dimensions of the etching vias will be defined as design parameters in this study. Figure 8 indicates the FEM models with etching via of 10µm, 20µm and 30µm. The stress free condition of the FEM analysis was defined at room temperature of 25°C. The loading condition was 10psi pressure loading at the input voltage 5 volts. Figures 9 and 10 show the x-direction stress distribution of the novel structure sensor with 10µm and 20µm etching via diameters, respectively. The stress concentration zone was located at the edge of the membrane, where the resistors were implanted. Figure 11 illustrates the relationship between the output voltage and the etching via diameters (10µm, 20µm and 30µm) of the novel pressure sensor. It could be observed in Fig. 11 that as the diameter of the etching via increased, the output voltage of the novel sensor increased. This phenomenon was due to the fact that, as the diameter of the etching via increased, the structure

of the silicon membrane becomes more compliant, and the stress at the concentration zone of the silicon membrane increased. Therefore, by applying equation (6), it could be found that the larger stress on the piezoresistors, the higher output voltage of the Wheatstone-bridge. According to the above result, increasing the diameter of the etching via could enhance the output voltage and the sensitivity of the pressure sensor. However, for the purpose of fabrication, a larger etching via may cause an imperfect polyimide coating coverage. Therefore, the designer should keep a balance between the output signal enhancement and the fabrication process.

The horizontal line in Fig. 11 shows the output voltage of the conventional pressure sensor. It was found that the output voltage of the novel structure pressure sensor was higher than that of the conventional one under the same pressure loading. This indicated that the novel structure pressure sensor had a high sensitivity. It also confirmed that the pressure sensor applied novel etching via fabrication process was feasible for the membrane type micro-sensor application.



Fig. 9 The silicon membrane x-directional stress distribution of novel structure sensor with 10 µ m etching via



Fig. 10 The silicon membrane x-directional stress distribution of novel structure sensor with 20 μ m etching via



Fig. 11 The output voltage variation of the novel pressure sensor with etching via (diameter =10 μ m, 20 μ m and 30 μ m)

• Packaging effect of the novel structure pressure sensor

The packaging effect that will influence the sensor stability is another significant design consideration of the novel structure pressure sensor. The novel sensor is comprised several materials such as polyimide thin film, silicon chip, adhesive layer and PCB substrate. Thereby, the CTE (Coefficient of Thermal Expansion) mismatch between different materials will cause the package-induced thermal stress as temperature changes and hence induce the sensor output voltage variation. For the above reason, the design parameters including the thickness of adhesive layer and the material property of polyimide were performed in this research to study the packaging and thermal effect of the packaged sensor due to temperature and pressure loading. The loading condition of the FEM analysis was 10psi pressure loading at temperature of 60° C, and the input voltage was 5 volts. Because of the focus in this section is the package-induced stress, the temperature coefficient of piezoresistance was set to be compensating with temperature coefficient of resistance (TCR) in the fabrication process.



Fig. 12 The silicon membrane x-directional stress distribution of the novel structure sensor with 10µm etching via diameters under temperature and pressure loading

A. Material property of polyimide

Figure 12 indicates the x-direction stress distribution of the novel structure sensor with 10 μ m etching via diameters under temperature and pressure loading. Due to the thermal effect between different materials of the novel structure sensor, the x-direction stress in Fig. 12 varies as comparing with it in Fig.8. The stress variation during temperature loading will cause the output voltage instability of the sensor. Figure 13 illustrates the relationship between the output voltage and the etching via diameters at 25°C (room temperature) and 60°C. It could be found in fig. 13 that the sensor output voltage varies during temperature changing. This output voltage variation will cause the non-linearity of the sensor output signal, and it will be severer as the thermal loading increases.



Fig. 13 The output voltage variation of the novel pressure sensor with etching via under different temperatures

In order to reduce the sensor signal instability resulting from CTE mismatch, a lower CTE polyimide is applied in the analysis. Figure 14 depicts the output voltage variation versus the polyimide with different CTE (20ppm and 30ppm) during temperature loading. In Fig. 14, it is found that the polyimide with lower CTE can reduce the output voltage variation under thermal loading, and hence the stability of the novel pressure sensor could be enhanced. This is due to the fact that the CTE of lower CTE polyimide (20ppm) is closer to that of silicon (2.62ppm), thereby the thermal stress between silicon and polyimide could be degraded.

B. Thickness of adhesive layer

Another design concept to reduce the thermal effect of the packaged sensor is applying a thicker adhesive layer as a buffer to absorb the thermal stress between silicon and PCB board. Figure 15 indicates the adhesive layer thickness versus the output voltage variation. The thickness of adhesive layer is varied from $50 \,\mu$ m to $100 \,\mu$ m. Referring to this figure, the output voltage of the novel sensor with $50 \,\mu$ m adhesive layer thickness up to $100 \,\mu$ m, the output voltage variation almost vanishes. Thus confirming that a thicker adhesive layer shows a better buffer effect to the package-induced thermal stress, and accordingly upgrades the sensor output signal stability. Moreover, comparing the findings in Fig. 14 and Fig. 15, it

could be observed that increasing the thickness of adhesive layer elevates more sensor output signal stability than reducing the CTE of polyimide does.



Fig. 14 The output voltage variation versus the polyimide with different CTE (20ppm and 30ppm) during temperature loading



Fig. 15 Adhesive layer thickness versus the output voltage variation during temperature loading

VII. Conclusion

By applying etching via technology, this study studied and developed a novel fabrication process of silicon base piezoresistive pressure sensor. As far as the fabrication process is concerned, the etching via technology successfully accomplished a front-side etching process to replace the conventional back-side etching process. By applying the etching via technology proposed in this investigation, the novel structure pressure sensor could reduce the chip size by at least 50% over the conventional one. The chip size reduction of the novel sensor could elevate the sensor chip counts per wafer and thereby reduce the manufacturing cost. Furthermore, according to the FEM comparison results, it was found that the novel structure pressure sensor showed better sensitivity than the conventional one. On the other hand, the packaging design consideration of the novel sensor in this study indicates that the thicker thickness of adhesive layer and the lower CTE of polyimide material can upgrade the sensor signal stability under temperature loading. Therefore, it can be concluded that due to

the size reduction, the sensitivity enhancement and the linearity elevation, this sensor not only applies to more advanced applications, but also shows a cost advantage in the fabrication process.

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