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DESIGN AND ANALYSIS OF THE CMOS COMPATIBLE PRESSURE SENSOR USING FLIP CHIP AND FLEX CIRCUIT BOARD TECHNOLOGIES

Chih-Tang Peng[1], Chang-Chun Lee[1], Kuo-Ning Chiang[2]

E-Mail: Knchiang@pme.nthu.edu.tw

Department of Power Mechanical Engineering

National Tsing Hua University

HsinChu, Taiwan 300, R.O.C.

Abstract

In this study, a silicon base piezoresistive pressure sensor using flip chip and flex circuit packaging technologies is studied, designed and analyzed. A novel designed pressure sensor using flip chip packaging with spacer is employed to substitute the conventional chip on board or SOP packaging technology. Subsequently, a finite element method (FEM) is adopted for the designing of the sensor performance. Thermal and pressure loading is applied on the sensor to study the system sensitivity as well as the thermal and packaging effect. The performance of novel packaging pressure sensor is compared with that of the conventional one to demonstrate the feasibility of this novel design. The findings depict that this novel packaging design can not only maintain well sensor sensitivity but also reduce the thermal and packaging effect of the pressure sensor.

Keywords: Piezoresistive pressure sensor, finite element method (FEM), Package and flip chip.

I. Introduction

Nowadays, silicon piezoresistive pressure sensor is a mature technology in industry. Certainly, the sensor stability after packaging becomes more significant for the high-precision pressure sensor design consideration. Thereby, this study presents a silicon base piezoresistive pressure sensor using flip chip and flex circuit packaging technologies to reduce its thermal and packaging effect. Figure 1 indicates a conventional DIP packaging pressure sensor. Figure 2 depicts the drawing of a novel pressure sensor using flip chip and flex circuit packaging.

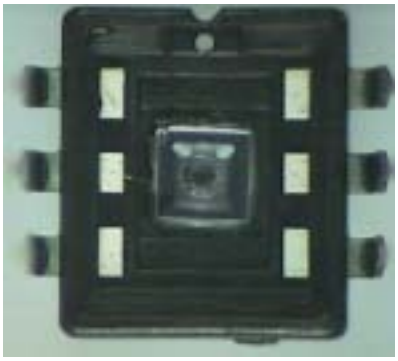


Fig. 1 The conventional DIP packaging pressure sensor
Reference: NAIS, ADP1131

[1]. Graduate Assistant, Ph.D candidate
[2]. Corresponding Author, Professor, Dept. of Power Mechanical Engineering, National Tsing Hua University

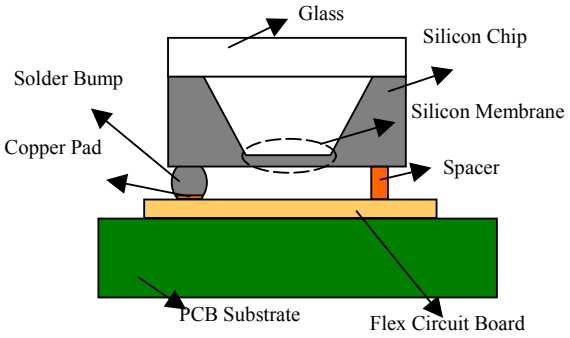


Fig. 2: The drawing of flip chip type pressure sensor

The fundamental concept of piezoresistive effect is the change in resistivity of a material causing from an applied stress. This effect in silicon material was first discovered by Smith [1] in 1950's and was applied extensively in mechanical signal measurement for years. Smith proposed the change in conductivity under stress in bulk n-type material and designed an experiment to measure the longitudinal as well as transverse piezoresistance coefficients. Pfann [2] presented the shear piezoresistance effect, he designed several types of semiconductor stress gauge to measure the longitudinal, transverse, shear stress and torque, and a Wheastone bridge type gauge is employed in mechanical signal measurement. Piezoresistance coefficient is a function of impurity concentration and temperature; hence the thermal effect will influence the measurement result of a piezoresistive sensor. Kanda [3] produced a piezoresistance coefficient study about orientations, impurity concentration and temperature. Lund [4] also studied the temperature dependency of piezoresistance coefficient by four points bending experiment.

Piezoresistive pressure sensor design is widely studied at 1990's in MEMS and electronic packaging field. Jaeger et al. [5, 6] employed piezoresistive sensor made on silicon chip to measure the stresses within electronic packaging devices. Kanda [7] applied MEMS process to fabricate piezoresistive pressure sensors on {100} and {110} wafer for optimum design considerations.

Recently, the finite element method (FEM) is widely adopted for stress prediction, thermal effect reduction, packaging design and reliability enhancement of piezoresistive sensor. Pancewicz [8] used FEM to obtain the output voltage of the pressure sensor and compared the simulation data with experiment result. Schilling [9] also applied FEM analysis for sensor performance simulation and discussed the packaging effects on silicon piezoresistive pressure sensors. However, some design parameters such as packaging material and packaging structure that could influence the sensor stability were not discussed.

Ⅱ. Fundamental theory of piezoresistive pressure sensor

The piezoresistive effect is the change in resistivity of a material due to an applied load. The piezoresistive influence on the stress state of the doped silicon wafer had been discussed by several researches [1], [2], [3], [10]. In this section, the mathematical relation between the piezoresistance and the output voltage of the pressure sensor will be introduced. Moreover, the introduced equations will be applied to finite element analysis.

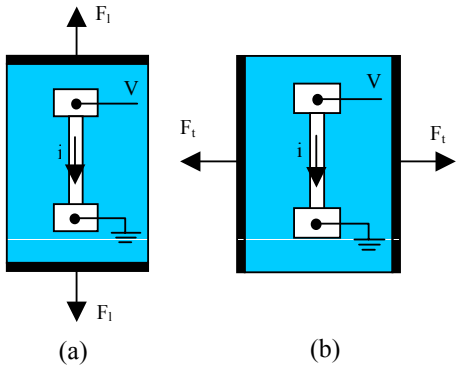


Fig.3: The force/current situations that rules by (a) the longitudinal piezoresistance coefficient and (b) the transverse piezoresistance coefficient

For a membrane type piezoresistance pressure sensor, the stress state on the resistors can be assumed to be plane stress ($\sigma_z=\sigma_{xz}=\sigma_{yz}=0$) condition and the shear stress σ_{xy} << the normal stress σ_x, σ_y. The most common situation of the piezoresistors under force loading is schematically in Fig. 3. In Fig. 3(a), considering a longitudinal force F_l and a voltage V are applied on the piezoresistor. The uniaxial stress, electric field and current of this piezoresistor are all in the same direction (this direction not necessarily along a crystal axis). In Fig. 3(b), considering a transverse force F_t and a voltage V are applied on the piezoresistor. It could be found in fig. 3(b) that the uniaxial stress is in perpendicular to the direction of electric field and current. Therefore, two uniaxial stresses are defined: a longitudinal stress, σ_l and a transverse stress, σ_t for the membrane type piezoresistance sensor application.

The relationship between resistivity variations and stress changes can be expressed as follows (Equation 1):

$$\Delta\rho/\rho = \pi_l\sigma_l + \pi_t\sigma_t \tag{1}$$

$$\pi_l = \pi_{11} + 2(\pi_{44} + \pi_{12} - \pi_{11})(l_1^2m_1^2 + l_1^2n_1^2 + m_1^2n_1^2) \tag{2}$$

$$\pi_t = \pi_{12} - (\pi_{44} + \pi_{12} - \pi_{11})(l_1^2l_2^2 + m_1^2m_2^2 + n_1^2n_2^2) \tag{3}$$

Where π_l is the longitudinal piezoresistance coefficient and π_t is the transverse piezoresistance coefficient. π_{ij} are the piezoresistance coefficients defined as a six by six matrix. For the cubic crystal structure of silicon, due to the symmetry conditions, the coefficients of matrix can reduce to three independent components: π_{11}, π_{12}, and π_{44}. l, m and n are the direction cosines between the <100> axis and a given crystal direction.

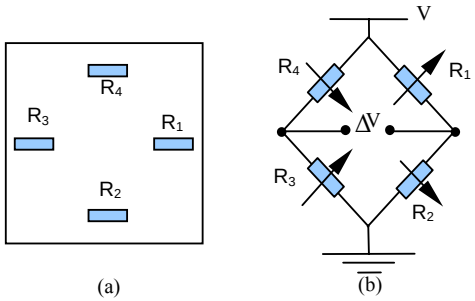


Fig. 4 (a) Four piezoresistors on a membrane (b) Wheatstone bridge configuration of the four piezoresistors

Figure 4(a) illustrates a membrane with four piezoresistors. If the resistors are correctly positioned on the membrane, the change in resistance of the first two piezoresistors will be opposite to that of the other two. Therefore the absolute value of the four-resistance variation can be equal. The resistors are connected in a Wheatstone bridge as shown in Fig. 4(b), where V_{in} is bridge-input voltage, and ΔV is the differential output voltage. The resistance change due to an unbalanced bridge can directly convert into a voltage signal under an applied pressure. For ΔR<< R, Equation (4) indicates the voltage and resistance relationship:

$$\Delta V = \frac{r}{(1+r)^2}\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2} + \frac{\Delta R_3}{R_3} - \frac{\Delta R_4}{R_4}\right)V_{in} \qquad (4)$$

Where $r = \frac{R_2}{R_1} = \frac{R_3}{R_4}$, ΔR_i is the i^{th} resistance change, R_i is the i^{th} zero-stress resistance.

For $R = |R_1| = |R_2| = |R_3| = |R_4|$ in equation 4, the mechanical stress, the total resistance change (ΔR) and the output voltage relation, which neglect the dimensional changes, can be expressed as follows:

$$\frac{\Delta V}{V_{in}} = \frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} = \sigma_l \pi_l + \sigma_t \pi_t \qquad (5)$$

The mechanical stresses obtained by FEM should be transferred into output voltage in such a way that the simulation stress value can be applied to predict the equivalent output electrical signal. Equation (6) indicates the output voltage, resistance and stress variation relation [11]:

$$\frac{\Delta V}{V_{in}} = \frac{\Delta R}{R} = \frac{\pi_l(\sum_{i=1}^{n}\sigma_{li}v_i) + \pi_t(\sum_{i=1}^{n}\sigma_{ti}v_i)}{\sum_{i=1}^{n}v_i} \qquad (6)$$

Where i is the piezoresistive element number of the finite element model, σ_{li} and σ_{ti} are the longitudinal and transverse stresses of the i^{th} piezoresistive element, respectively, and v_i is the volume of the i^{th} element on the piezoresistors. Figure 5 indicates the piezoresistors on the quarter of finite element model. By applying this transfer method, the FEM simulation can be employed to predict the output voltage of the piezoresistive pressure sensor.

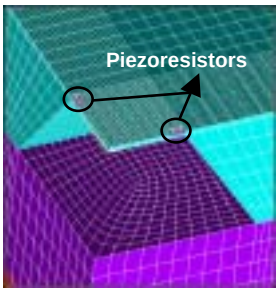
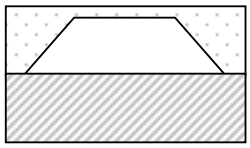


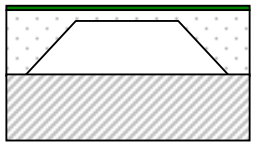
Fig. 5: Piezoresistors on the quarter of finite element model

Ⅲ. The packaging fabrication process of the novel flip chip pressure sensor

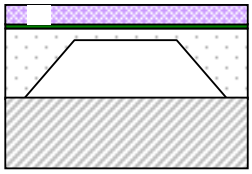
The packaging fabrication process comprises several steps shown in figure 6(a) to figure 6(e). First, in figure 6(a), a wafer with the pressure sensor chip that was fabricated by the CMOS compatible process as well as the bulk micromachining (electrochemical backside etching) process [11] is bonded with a glass layer to form a sealing chamber. Figure 6(b) illustrates the UBM sputtering process. Follows, an electroplating process is employed to fabricate the eutectic solder layer (shows in figure 6(c) and figure 6(d)). In figure 6(e), the photoresist as well as the UBM layer are stripped and the eutectic solder is reflowed to form the solder bumps. Finally, after wafer slicing, the pressure sensor chip is mounted with a flex circuit board mounted on a PCB substrate (shows in figure 6(f)). There are some copper spacers bonding on the flex circuit board to support the silicon sensor chip. After the above fabrication process, this pressure sensor using flip chip and flex circuit packaging technology is completed.



The wafer bonding with glass
6(a)



UBM layer sputtering on the wafer
6(b)



PR coating and pad patterning
6(c)

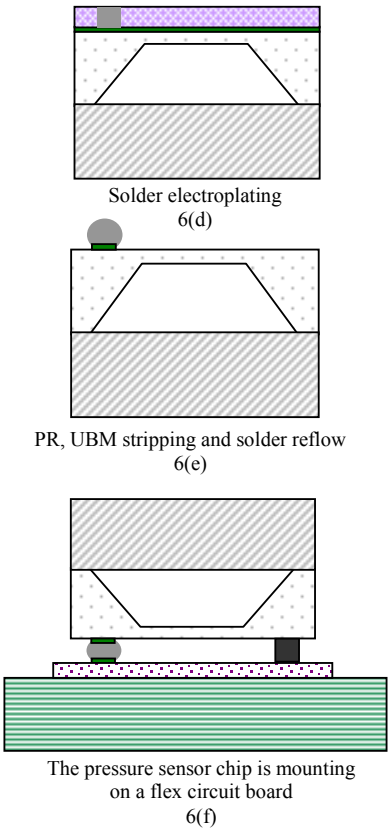


Fig. 6: The packaging fabrication process of the novel flip chip pressure sensor

Ⅳ. Finite element models

In order to validate the feasibility of the novel packaging type pressure sensor, a performance comparison between the conventional and novel packaging type pressure sensor is inevitably. According to the previous research [11], the FEM analysis that can predict the mechanics output signal of the pressure sensor accurately is demonstrated. Consequently, the finite element method was adopted to simulate the mechanical behaviors of the conventional chip on board pressure sensor and the novel flip chip packaging pressure sensor. In this study, the commercial software ANSYS^{R} was applied to analyze mechanical signal change due to thermal and pressure loading. The FEM models of the conventional chip on board pressure sensor and the novel flip chip packaging pressure sensor were described as follows:

- *The FEM model of the conventional chip on board pressure sensor:*

Figure 7 illustrates the structure cross-section and the top view of the conventional chip on board packaged pressure sensor. The quarter finite element model of the conventional packaged pressure sensor was established in Fig. 8, since the packaged pressure sensor device is quartered symmetry.

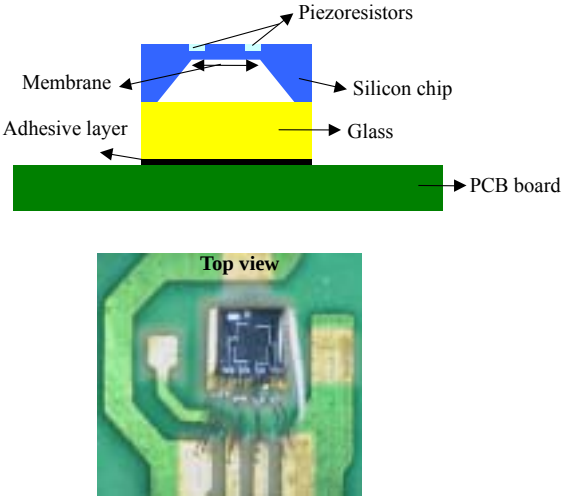


Fig. 7: The structure cross section and top view of the packaged pressure sensor

The finite element model of conventional pressure sensor comprises silicon chip, adhesive, glass and PCB substrate. The model contains 23,450 eight-node 3D elements and 79,614 D.O.F. The boundary conditions of the center surfaces are: x-directional displacement is fixed on the y-z plane, y-directional displacement is fixed on the x-z plane, and all nodes on the bottom side of PCB substrate are fixed in x, y, and z directions. The ambient temperature and stress free temperature was assumed at 25^{0}C. Table 1 lists the dimensions of PCB, glass, adhesive layer, silicon chip and silicon membrane.

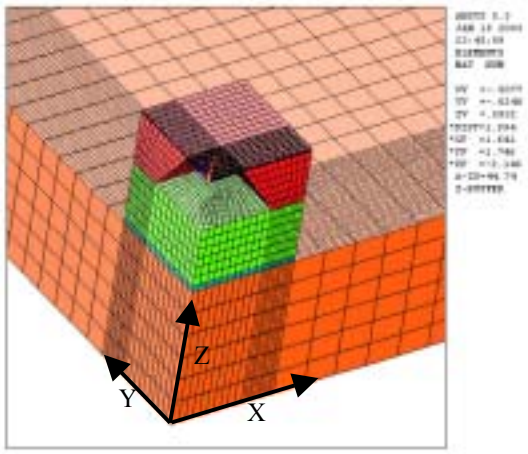


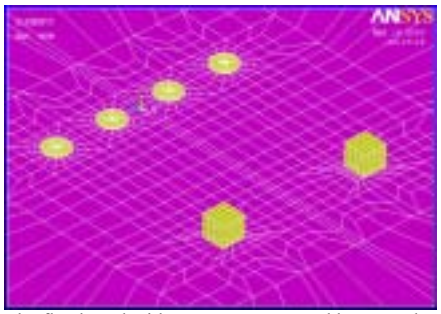
Fig. 8: One-quarter finite element model of piezoresistive pressure sensor

Table 1. Dimensions of PCB, glass, adhesive layer, silicon chip and silicon membrane

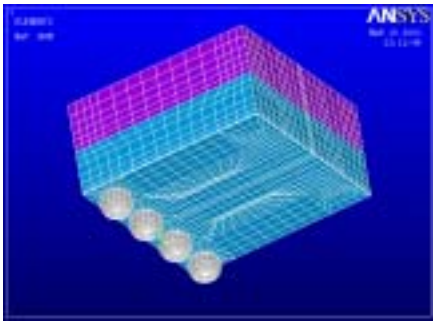
	Length (μm)	Width (μm)	Thickness (μm)
PCB	10000	10000	1200
Glass	1800	1800	500
Adhesive	1800	1800	50
Silicon Chip	1800	1800	450
Silicon Membrane	600	600	20

- *The FEM model of the novel flip chip packaging pressure sensor:*

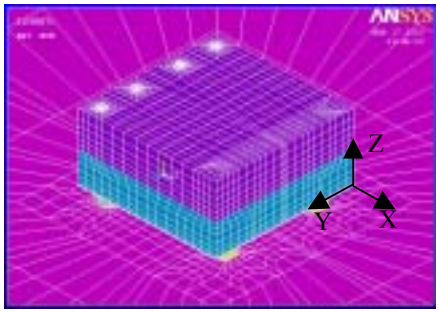
The novel structure pressure sensor comprises glass, silicon chip, solder ball, flex board and PCB substrate. A full-scale three-dimensional finite element model that contains eight-node 3D elements and D.O.F. was established. Figure 9 indicates the finite element model of the novel flip chip packaging pressure sensor. Figure 9(a) depicts the flex board with two copper spacers and bump pads on it. Figure 9(b) shows a glass bonding with a sensor chip where the solder bump is fabricated. In figure 9(c), it is observed that the silicon chip is assembled on the flex board. The solder bumps interconnect the silicon chip and the flex board, and the spacers are utilized as supports to keep silicon chip remaining horizontal after the chip flips on the flex board. Figure 9(d) shows the structure of the silicon sensor chip. The cross-section view of this novel flip chip packaging pressure sensor is illustrated in figure 9(e). The dimension of the spacer is 100 μ m x 100 μ m x 200 μ m. The standoff height of the solder bump is 200 μ m, and the bump pads on die side as well as on flex board side are both 200 μ m.



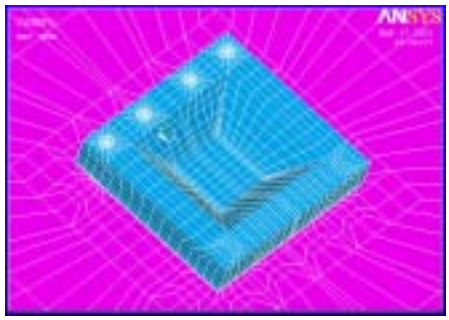
The flex board with copper spacers and bump pads
9(a)



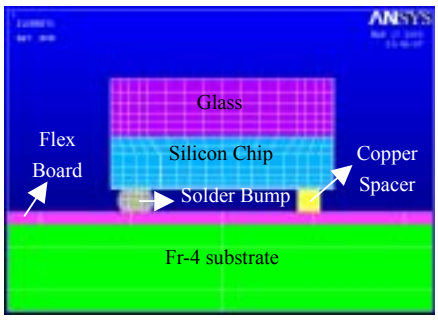
The glass bonding with the sensor chip
9(b)



The sensor chip assembly on the flex board
9(c)



The structure of the pressure sensor
9(d)



The cross-section of the novel packaging pressure sensor
9(e)

Fig. 9: The finite element model of the novel flip chip packaging pressure sensor

The boundary condition of this novel packaged sensor is the bottom side fixed in x, y and z directions. The ambient temperature and stress free temperature was assumed at 25^0C. In order to release the packaging induced thermal stress between different materials due to CTE mismatch (Coefficient of Thermal Expansion) as temperature varies, the flex board is not fully bonded with the PCB substrate but sets to be suspended on the PCB substrate with one side adhered with the PCB substrate by solder bumps. Owing to this design concept, the contact behavior will occur between spacers/silicon chip and flex board/PCB substrate consequently. Thereby, the 3D four-nodes surface contact pair elements are employed on the spacers/silicon chip and flex board/PCB substrate for the contact physical phenomena simulation between these two interfaces.

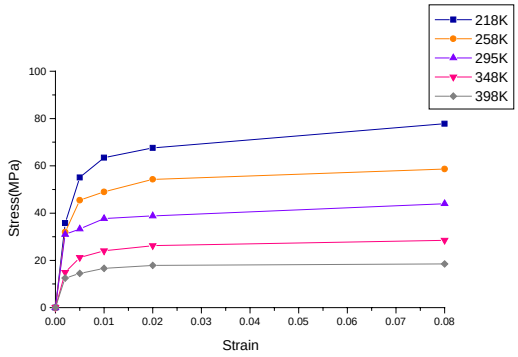


Fig. 10: Nonlinear material properties of solder (60Sn/40Pb)

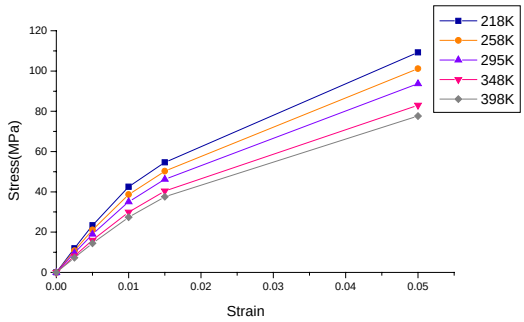


Fig. 11: Nonlinear material properties of polyimide

Table 2 lists the dimensions of PCB, glass, silicon chip, flex board and silicon membrane. Table 3 indicates the material properties of PCB (FR-4), glass (7740), adhesive layer, silicon, copper (spacer and bump pad), solder bump and flex board (polyimide). Figure 10 and 11 illustrate the nonlinear material properties of solder (60Sn/40Pb) and polyimide, respectively.

Table 2. Dimensions of PCB, flex board, glass, silicon chip and silicon membrane

	Length (μm)	Width (μm)	Thickness (μm)
PCB	5800	5800	1200
Flex Board	2800	2800	100
Glass	1800	1800	500
Silicon Chip	1800	1800	450
Silicon Membrane	600	600	20

Table 3. Material properties of PCB (FR-4), glass (7740), adhesive, silicon, copper, solder bump and flex board

	Young's Modulus (Gpa)	Poisson's Ratio	CTE (1/℃)
PCB (FR-4)	18	0.19	16ppm
Glass (7740)	76	0.28	3.25ppm
Adhesive	8.96	0.25	15ppm
Silicon	112.4	0.28	2.62ppm
Copper	117	0.31	17ppm
Solder (60Sn/40Pb)	Temperature Dependent	0.35	23.9ppm
Flex Board (Polyimide)	Temperature Dependent	0.34	40ppm

Ⅴ. Results and discussions

The major factors of a pressure sensor performance are sensor output signal sensitivity and stability. To validate this novel sensor packaging design, the sensitivity and stability comparisons between the conventional and novel packaging type pressure sensor are accomplished.

- *The sensor sensitivity comparison between the conventional chip on board pressure sensor and the novel flip chip packaging pressure sensor:*

In order to study the sensitivity between the conventional chip on board pressure sensor and the novel flip chip packaging pressure sensor, the loading condition of pressure 10psi is applied on the surface of the sensor chip, and the input voltage is set to be 5 (Volts).

The longitudinal and transverse piezoresistance coefficients in this study are $\pi_l = 1/2(\pi_{11}+\pi_{12}+\pi_{44})$ and $\pi_t = 1/2(\pi_{11}+\pi_{12}-\pi_{44})$, where $\pi_{11} = 6.6*10^{-11}$ (Pa^{-1}), $\pi_{12} = -1.1*10^{-11}$ (Pa^{-1}), and $\pi_{44} = 138.1*10^{-11}$ (Pa^{-1}) (p-type silicon at low doped value and room temperature condition, ref. [1]).

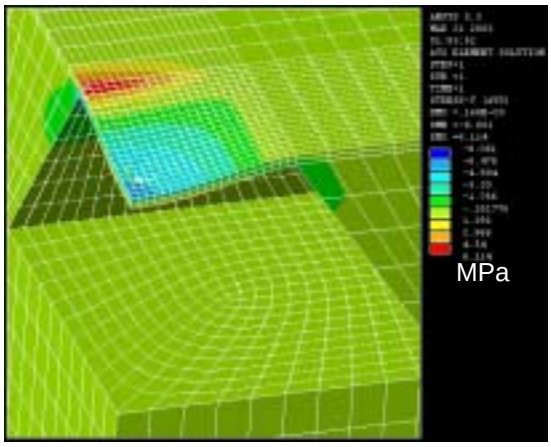


Fig.12: The Y-directional stress of the conventional chip on board pressure sensor

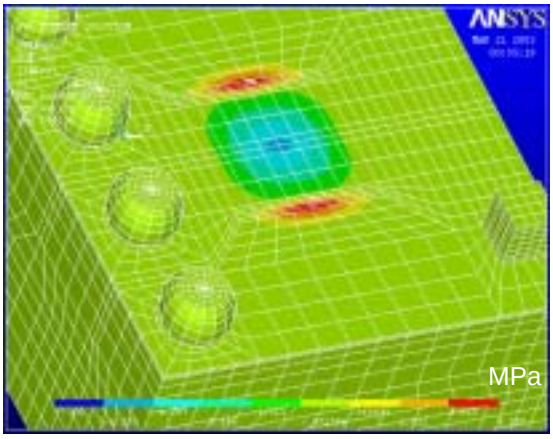


Fig.13: The Y-directional stress of the novel flip chip packaged pressure sensor

Figure 12 and 13 indicate the Y-directional stress of the conventional sensor and the novel sensor, respectively. It is observed in these two figures that the maximum stress is located on the center of the silicon membrane edge where the piezoresistors are implanted.

Since the longitudinal and the transverse stresses (X and Y directional stress) are obtained, the output voltage can be calculated by equation (18). The output voltage of the novel flip chip packaged sensor at 10psi pressure loading is **11.16** (mVolts), and that of the conventional chip on board sensor is **11.24** (mVolts). The result indicates that the novel pressure sensor shows the competed output signal sensitivity with the conventional one. Thus confirms the feasibility of the novel packaged sensor in terms of the output signal sensitivity.

● *The sensor stability comparison between the conventional chip on board pressure sensor and the novel flip chip packaging pressure sensor:*

By employing the flex board technology, this investigation intends to reduce the packaging induced thermal stress that causes the instability of the sensor output signal. Therefore, in order to discuss the functionality of this flex circuit board design, a 10psi pressure loading is applied on the novel and conventional sensors while the temperature is varied from -10^0C to $+60^0$C to achieve a output signal stability comparison between these two sensors. The input voltage is set to be 5 (Volts).

Figure 14 depicts the stability comparison result between the novel sensor and the conventional sensor. In fig. 14, the output voltage linearity of the novel flip chip packaged sensor is better than that of the conventional chip on board one. Therefore, it could be concluded that the novel sensor upgrades more output signal stability than the conventional one. This is due to the fact that the different materials within sensor structure cause thermal stress owing to CTE mismatch as temperature varies, thus influence the output signal stability. However, the suspended flex board design can release most of the packaging induced thermal stress between different materials due to CTE mismatch as temperature varies. Based on the above finding, this novel sensor using flip chip and flex board packaging proposed in this study indeed provides a more stable output signal quality.

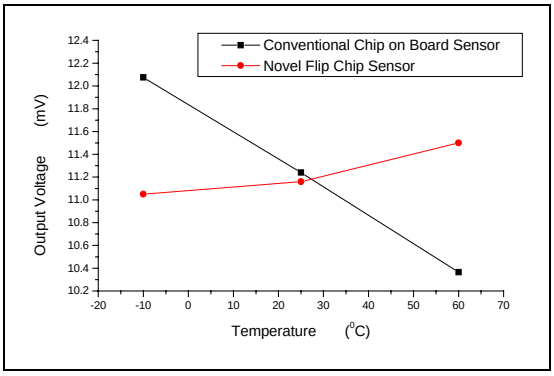


Fig. 14: The stability comparison result between the novel sensor and the conventional sensor

VI. Conclusions

This investigation studied and developed a novel packaging type silicon base piezoresistive pressure sensor by applying flip chip and flex board technologies. According to the FEM comparison results of sensor signal sensitivity and stability, it is found that the novel packaging type pressure sensor not only shows a competed sensitivity but also provides a better stability as comparing it with the conventional one. Thereby demonstrates the feasibility of the novel packaging design. Furthermore, as far as the packaging process is concerned, this novel sensor employs the electronic package industry compatible process. Thus the fabrication of this novel flip chip packaging pressure sensor could accomplish easily. Based on the above reasons, this novel packaged pressure sensor can be applied in the advanced application that needs stability enhancement and sensitivity maintenance of the sensor performance.

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