Design, Fabrication and Comparison of Lead-Free/Eutectic Solder Joint Reliability of Flip Chip Package

Chih-Tang Peng[1], Kuo-Ning Chiang[2], Terry Ku[3], Kenny Chang[3]
Corresponding Author: Knchiang@pme.nthu.edu.tw
Department of Power Mechanical Engineering
National Tsing Hua University
HsinChu, Taiwan 300, R.O.C.

Abstract

Flip chip technology provides many benefits, including high I/O connections, high electrical performance, and high reliability. As a result it has attracted a great deal of attention in the area of advanced electronic packaging. At the same time, an ever increasing need has developed for a lead-free flip chip interconnection due to the restrictions on the use of lead, and the upward spiraling market demand for green products. For these reasons, this investigation presents a detailed design procedure for a lead-free flip chip BGA package which includes solder bump profile prediction, finite element method (FEM) simulation, test vehicles design/fabrication and acceleration thermal cycle (ATC) testing to study the reliability issues of the flip chip packages. The solder joint reliability of a flip chip package depends on the solder materials and the solder geometry that includes solder volume, die-side pad and substrate-side pad dimensions, etc. Therefore, this study is divided into two main topics: one is the effect of solder joint material (eutectic 63Sn/37Pb solder and lead-free 96.5Sn/3.5Ag solder) on the solder joint reliability, and the other is the effect of the geometry on the Sn/Ag solder joint reliability. In order to achieve both these goals, a test vehicle design procedure is developed as follows: First, a force-balanced analytical approach is applied for the solder joint profile prediction. Then, a finite element method (FEM) is adopted for the test vehicle reliability analysis. Subsequently, the validity of the FE modeling is demonstrated extensively through typical accelerated thermal cycling (ATC) testing. To facilitate the testing, five different test vehicles of the fine-pitch flip chip BGA packages, including the daisy chain circuit, are designed and fabricated for electrical resistance measurement. The results show that the test vehicle of the flip chip package utilizing lead-free 96.5Sn/3.5Ag solder indicates a better solder joint reliability than when utilizing eutectic 63Sn/37Pb solder. In terms of the lead-free solder joint geometry design, the solder joints of the test vehicle with a higher standoff height and a larger solder volume shows a better solder joint reliability, and in addition, the trends of the ATC testing coincide with the FE analysis results, thus confirming that this analysis-fabrication procedure is feasible for the solder joint geometry and material design of a flip chip BGA package.

Keywords: **Lead-free solder, Flip chip BGA, Acceleration thermal cycling, Daisy chain, Finite element method.**

1. INTRODUCTION

Flip chip technology is being widely used in current electronics packaging industry due to its better thermal performance, smaller size, lower profile, lighter weight, and higher I/O density. In a flip chip package, the solder joints, together with underfill, serve as a mechanical mechanism for resisting the thermal deformation induced by the CTE mismatch between the silicon die and the substrate.

The key factors that influence solder joint reliability include the geometry of the solder joints, underfill material, solder material, as well as package's layout and structure. Once the package's layout and structure, underfill and solder materials are determined, the geometry of the solder joint dominates the fatigue life of the package. Thus, it becomes essential to establish the geometry of the solder joint prior to performing solder joint reliability prediction. Basically, solder joint geometry, such as standoff height, lower/upper contact angles of solder joints, and solder joint profile etc., are determined by the solder volume applied, the die/substrate-side pad size and the surface tension force of the molten solder during the reflow process. In the literature, various types of technologies have been applied to predict the geometry of solder joints after solder paste reflow. For example, Heinrich et al. [1] and Chiang and Chen [2] applied a force-balanced analytical algorithm to predict the geometry of area array typed solder joints, and Pfeifer [3] proposed a geometry-based algorithm, i.e., the so-called truncated sphere method, to predict the solder joint shape, which does not take into account any force or energy factors. In essence, these approaches were generally considered effective and reliable for making the shape prediction of solder joints associated with a round pad.

Many studies on solder joint reliability in the flip chip technology have been extensively reported in literature. For examples, Liu and Chiang [4] and Chiang et al. [5] found that solder joint reliability is highly

[1]. Graduate Assistant, Ph.D candidate
[2]. ***Corresponding Author***, Professor, Dept. of Power Mechanical Engineering, National Tsing Hua University/Electronics Research and Service Organization, Industrial Technology Research Institute, HsinChu, Taiwan
[3]. VIA Technology Corporation, Taiwan

depending on solder joint geometry, such as their standoff height, lower/upper contact angles of solder joints, and solder joint profile etc. Mercado [6, 7] performed FE parametric analysis of the reliability of flip chip PBGA packages with respect to the many design parameters, including solder bump layout, solder bump center to die edge, solder material/geometry, die size as well as substrate size/material. Rosner et al. [8] conducted a thermal cycling test for reliability characterization of the flip chip packaging using isotropically conductive adhesives. In their research, a special daisy chained test IC is designed for the packaging reliability testing, and the daisy chain electrical resistance variation is measured at different time instances during the thermal cycling. The results indicate that the package's structural failure may occur at both low and high temperatures in thermal cycling.

At the same time, there is sharp rise in demand for a lead-free flip chip interconnection due to the restrictions on lead usage, and the ever increasing demands of the market place for 'green' products. As a result, lead-free solder joint reliability studies have attracted a great deal of attention lately. Hou et al. [9] presented a Sn/Ag/Cu solder joint reliability study of flip chip packages. In their study, the assembly process for flip chip die with Sn/Ag/Cu solder bump is discussed, and thermal shock testing is applied for the Sn/Ag/Cu and Sn/Pb solder joint reliability testing. Their result indicates that the Sn/Pb solder shows a slightly better reliability. Zhang et al. [10] presented three lead-free solders: Sn/Cu0.7, Sn/Ag3.8/Cu0.7, Sn/Ag3.5 and one lead-containing solder: Sn/Pb37, on both electroless NiP and electroplated Cu under bump metallurgies (UBM) for flip chip applications. Based on the thermal cycling testing result in Hou's study, the Sn/Cu0.7 solder shows the best solder joint reliability among the four solders studied in their investigation and appears to be the best choice for a lead-free flip chip interconnect. Nevertheless, the reliability testing data of the lead-free solder joint between different literatures depict some variations. While one study may indicate lead-free solders show a better solder joint reliability than that of Sn/Pb solder, another article may very well present a contrary result. Therefore, the lead-free solder issues require further detailed study.

The underlying goal of the present study is to investigate the effects of the solder joint geometry, as well as material that influence the solder joint reliability of a fine-pitched FCBGA through FE modeling and experimental testing. To attain this objective, a fine-pitched FCBGA package with 735 I/Os is considered as the test vehicle. The test vehicle involves five different specimen designs of a solder joint in this investigation. Three of these designs utilizing 96.5Sn/3.5Ag lead-free solder are composed of different combinations of die/substrate-side pad size and solder volume, while the other two designs applied equivalent solder joint geometry, but adopted different solder material, 63Sn/37Pb solder and 96.5Sn/3.5Ag solder, respectively. The test vehicles are designed, fabricated and tested (ATC) for the reliability design. The flip chip is first mounted on a 1+2+1 built-up organic substrate, and subsequently, the flip chip package is assembled onto a testing, printed wiring board (PWB), by way of 664 BGA interconnects that are made of 63Sn/37Pb solder materials. A center cross-section of the flip chip BGA package is illustrated in Figure 1.

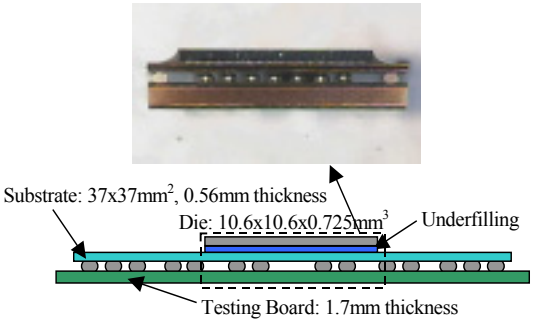


Fig. 1: Cross section view of flip chip BGA package

2. FLIP CHIP PACKAGE RELIABILITY DESIGN

In order to study the influence of the solder material and the solder bump geometry on the packaging reliability, five different package test vehicles: MPE005-1H, MPE006-1H, MPE007-1H, MPE005-1L and MPE005-2L were developed. Two test vehicles applied similar solder joint geometry but different solder material: MPE005-1L (utilizing 96.5Sn/3.5Ag solder) and MPE005-2L (utilizing 63Sn/37Pb solder) were built for the comparison of 63Sn/37Pb and 96.5Sn/3.5Ag solder joint reliability of a flip chip package. And, three test vehicles utilized identical solder material (96.5Sn/3.5Ag solder) but different combinations of die/substrate-side pad size and solder volume: MPE005-1H, MPE006-1H and MPE007-1H were employed for the effect of solder joint geometry on the solder joint reliability of a fine-pitched FCBGA.

2.1 Flip chip packaging solder joint shape prediction

The solder joint shape is first predicted by using the force-balanced method [1,2,11]. The solder joint geometry is subsequently used for the FE modeling, and for the preliminary assessment of the performance of solder joint reliability.

In this study, five different package test vehicles: MPE005-1H, MPE006-1H, MPE007-1H, MPE005-1L, and MPE005-2L are employed, as shown in Table 1.

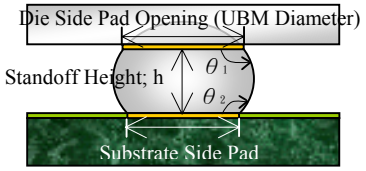
Table 1: The design parameters of five flip chip packaging test vehicles

Package Type	*MPE005-1H*	*MPE006-1H*	*MPE007-1H*	*MPE005-1L*	*MPE005-2L*
UBM Diameter	110 μm	120 μm	130 μm	110 μm	110 μm
Bump Height	91 μm	96 μm	99 μm	87 μm	84 μm
Substrate Side Pad Diameter	120 μm	120 μm	120 μm	120 μm	120 μm
Solder Material	96.5Sn/3.5 Ag	96.5Sn/3.5 Ag	96.5Sn/3.5 Ag	96.5Sn/3.5 Ag	63Sn/37Pb

The die size used in this investigation is 10.6mm x (g/mm^3), and the number of solder bumps is 735. The densities of 63Sn/37Pb solder and 96.5Sn/3.5Ag are 8.36 (gm/cm^3) and 7.36 (gm/cm^3), respectively. The surface tensions of 63Sn/37Pb solder and 96.5Sn/3.5Ag are 464 (dyne/cm) and 493 (dyne/cm), respectively. Based on the above data, the solder joint geometry can be predicted, and the results are shown in Table 2. It can be seen in Table 2 that MPE007-1H shows the highest standoff height and the largest solder volume and the smallest upper contact angle. As to the effect of solder joint material used on the solder joint reliability, MPE005-1L and MPE005-2L indicate a similar solder joint structure.

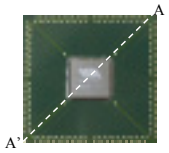
Table 2: *The prediction values of solder joint shape*

	Bump Volume (mm^3)	*Standoff Height On board (μm)*	*Width On Board (μm)*	*Upper Contact Angle, θ_1 (Degree)*	*Lower Contact Angle, θ_2 (Degree)*
MPE005-1H	0.000827	65.1	133.0	124.7	115.9
MPE006-1H	0.001006	71.5	140.2	121.6	121.6
MPE007-1H	0.001165	75.7	147.0	118.2	125.8
MPE005-1L	0.000762	61.2	131.1	123.4	114.1
MPE005-2L	0.000710	58.0	129.7	129.7	112.6
Substrate-Side Pad Diameter=120 μ m					

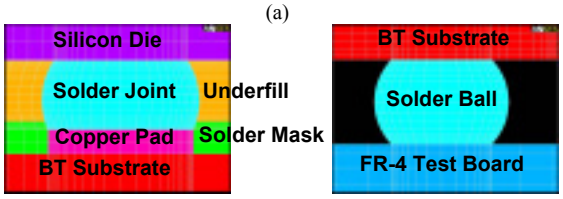


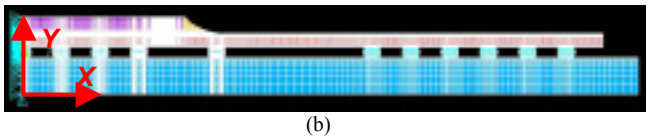
2.2 Finite element analysis

After the solder joint profile prediction, the finite element method (FEM) is applied in this study for the packaging reliability analysis. Five FEM models are employed in this study to simulate the accelerated thermal cycling (ATC), as well as temperature rise and dwell-time between -40°C and 125°C.



(a)





(b)

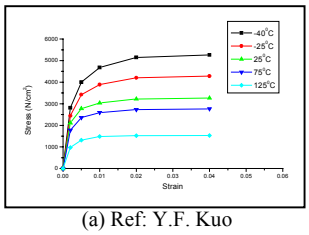
Fig. 2: Two-dimensional non-linear finite element model (MPE005-1H)

2.2.1 Finite element model

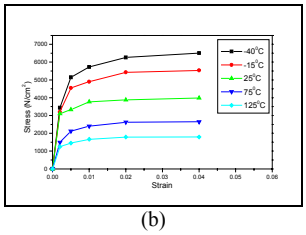
Numerical simulations of the thermal-mechanical behaviors of the test vehicle, subjected to thermal cycling loading, are performed in two-dimensional (2-D) plane 10.6mm x 0.725mm, the density of silicon is 2,330e-6 strain FE modeling. The 2-D plain strain FE analysis is carried out along the diagonal plane, which is the AA' cross-section shown in Fig.2 (a). All the main components of the FCBGA assembly are included in the FE models, including silicon chip, solder joints, BT substrate, copper pads on the substrate side, solder mask, underfill, BGA, and a PWB. Due to the symmetry of the package, only one half of the FCBGA package is modeled in the FE analysis. The symmetry boundary condition is imposed on the symmetry plane of the package, and the *y*-dir displacement at the bottom of the symmetry plane is constrained, in order to prevent it from rigid body motion during the FE analysis. Fig.2 (b) shows one example of the FE model associated with the MPE005-1H design. It consists of 64,500 elements with a total of 193,500 degree of freedoms (DOF). It should be noted that all the materials in the test vehicle are assumed to be linearly elastic, except those flip chip solder joints, BGAs and underfill, which are considered as a temperature-dependent and elasto-plastic material. Hence, the FE analysis also incorporates the temperature-dependent, non-linear plasticity into the modeling in order to characterize the inelastic stress/strain responses of solder joints. The material properties of these modeled components, including silicon chip, copper pad, FR-4 testing PWB, BT substrate and solder mask, are shown in Table 3, and the temperature-dependent, stress-strain relation of the solder joints (i.e. 63Sn/37Pb and 96.5Sn/3.5Ag) as well as the underfill are shown in Fig.3 and Fig.4, respectively. This study applied the commercial software ANSYS® to perform FE modeling and simulations. To ensure the convergence of the non-linear FE analysis, the full Newton-Raphson method is adopted in this investigation.

Table 3: Linear material properties of the FCBGA

Material	Young's Modulus (Gpa)	Poisson's Ratio	CTE (1/℃)
Silicon	112.4	0.28	2.62ppm
Copper pad	68.9	0.34	16.7ppm
FR-4 testing board	18	0.19	16ppm
BT substrate	9.92	0.20	15ppm
Solder mask	3.448	0.35	30ppm
Underfill	Non-linear	0.30	23.1ppm
96.5Sn/3.5Ag Solder	Non-linear	0.40	22.36ppm
63Sn/37Pb Solder	Non-linear	0.35	23.9ppm



(a) Ref: Y.F. Kuo



(b)

Fig. 3: The temperature dependent non-linear material properties of (a) Sn/Ag solder and Sn/Pb solder

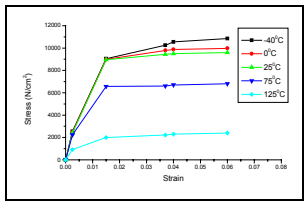


Fig. 4: The temperature dependent non-linear material properties of underfill

2.2.2 Thermal fatigue life prediction

As electronic packaging is subjected to temperature loading, the large stress/strain of a solder joint will cause a failure of the packaging structure. To predict the thermal fatigue life of the solder joint, the Coffin-Manson relationship [12] is employed.

Due to the fact that the stress acting on the solder joint of the flip chip package is not only dominant in the shear direction, the equivalent plastic strain is applied in this study. The incremental equivalent plastic strain can be expressed as:

$$d\varepsilon_{eq}^{pl} = \frac{\sqrt{2}}{3}\sqrt{(d\varepsilon_x^{pl} - d\varepsilon_y^{pl})^2 + (d\varepsilon_y^{pl} - d\varepsilon_z^{pl})^2 + (d\varepsilon_z^{pl} - d\varepsilon_x^{pl})^2 + \frac{3}{2}d\gamma^{pl}} \quad (1)$$

Where $d\gamma^{pl} = d\gamma_{xy}^{pl\,2} + d\gamma_{yz}^{pl\,2} + d\gamma_{zx}^{pl\,2}$ and $d\varepsilon_x^{pl}$ 、 $d\varepsilon_y^{pl}$ 、 $d\varepsilon_z^{pl}$ 、 $d\gamma_{xy}^{pl}$ 、 $d\gamma_{yz}^{pl}$ and $d\gamma_{xz}^{pl}$ are incremental plastic strain components acting on the solder bump.

Equation 2 indicates the summation of the incremental equivalent plastic strain in a stabilized cycle:

$$\Delta\varepsilon_{eq}^{pl} = \sum_{Cycle} d\varepsilon_{eq}^{pl} \quad (2)$$

Subsequently, the fatigue life of a eutectic solder can be predicted by an empirical Coffin-Manson relationship with Eq.2:

$$N_f = \theta(\Delta\varepsilon_{eq}^{pl})^{\eta} \quad (3)$$

Where the constants θ and η are modified to 0.4405 and –1.96, respectively.

3. DEVELOPMENT OF TEST VEHICLES

An ATC test is performed to explore the fatigue life of the flip chip solder joints and BGAs in the test vehicle. The obtained data, in terms of the fatigue life of flip chip solder joints and BGAs, are used specifically for benchmarking the modeled results.

3.1 Test vehicles

The test vehicle, the fine-pitch FCBGA package, is involved with five different types of solder joint structures; therefore, five different daisy chain test dies are designed and implemented. The bump pitch for the flip chip solder joints is 200 μm, and the distance of the die edge to the outmost solder bump center is 400 μm. In order to fulfill the resistance measurement during the ATC testing, a special daisy chain circuit has been designed and fabricated on both the BT substrate and the testing board, for substrate-level testing and board-level testing, respectively. In substrate-level testing, a daisy chain circuit is formed by one particular electrical route connecting all the flip chip solder joints. Similarly, in the board-level testing, the other specific electric route that chains all these BGA is designed, and is connected with the flip chip solder joints through the substrate.

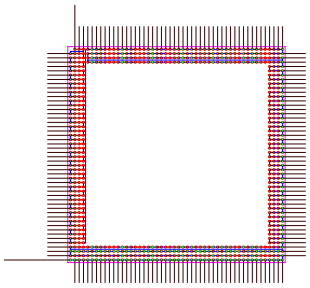


Fig. 5: Daisy chain circuit on flip chip solder joints (substrate level)

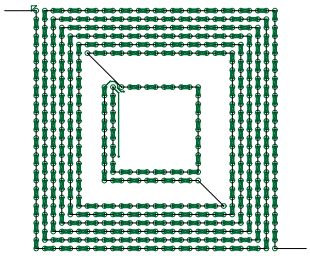


Fig. 6: Daisy chain circuit on BGAs (board level)

Fig.5 and fig.6, illustrate the designed daisy chain circuit layouts for both the substrate- and board-level testing, respectively. The test vehicle applies a 1+2+1 built-up organic (BT) substrate with a dimension of 37.5mm x 37.5mm x 0.56mm. The pad diameter for the BGA is 600 μm. Probing pads with a size of 500 μm x 500 μm are placed along the perimeter of the top side (i.e., flip chip side) of the substrate, and are shown in Fig. 8. These pads are connected with the outmost solder joints, and are applied to measure the signals of the outmost solder joints during the thermal cycling test, in order to locate the position of the solder joint in failure. The testing board is made of an organic material (i.e., FR-4), and its dimension is 210mm x 120mm x 1.70mm. It can accommodate six FCBGA packages for testing at the same time, as shown in Fig.9. The daisy chain network is formed once the die, substrate, and PWB are assembled together. The copper metal pads, the daisy chain circuit on the die side and the passivation layer are all patterned on the wafer. The UBM is composed of a layer of titanium (sputtered), copper (sputtered) and nickel (electroplated). Table 3 depicts the dimensions of the daisy chain line width, copper metal pad, passivation

opening and UBM opening of the test vehicles: MPE005-1H, MPE006-1H, MPE007-1H, MPE005-1L, and MPE005-2L. The die size of the test vehicles is 10.6mm x 10.6 mm, and the bump pitch is 200μm.

Table 3: The dimensions of the daisy chain line width, copper metal pad, passivation opening and UBM opening of test vehicles

	Daisy Chain Line Width (μm)	*Metal Pad Size (μm)*	*Passivation Opening (μm)*	*UBM Opening (μm)*
MPE005-1H	125	125	95	110
MPE006-1H	135	135	105	120
MPE007-1H	145	145	115	130
MPE005-1L	125	125	95	110
MPE005-2L	125	125	95	110

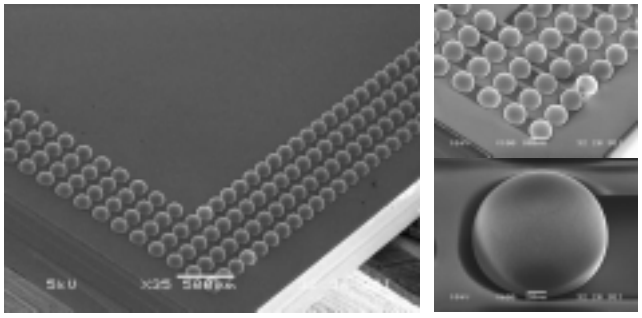


Fig. 7: The SEM photograph of the 96.5Sn/3.5Ag flip chip solder bump on a daisy chain wafer

The bump materials are 63Sn/37Pb solder on test vehicle MPE005-2L, and 96.5Sn/3.5Ag solder on test vehicles MPE005-1H, MPE006-1H, MPE007-1H and MPE005-1L. The material of the BGAs is 63Sn/37Pb eutectic solder. Fig.7 illustrates the SEM photographs of the solder bump on a daisy chain wafer.

3.2 Assembly

Prior to the assembly, a laminate BT substrate is fluxed, and subsequently, a die, diced from the wafer, is placed and aligned to the substrate by commercially available equipment. Then, the structure is reflowed by using a reflow oven to accomplish mechanical bonding. The peak temperature and the dwelling time are 220°C and 74sec for 63Sn/37Pb solder as well as 250°C and 78sec for 96.5Sn/3.5Ag solder, respectively. In order to reduce the thermal mismatch induced-stress on the solder joints, the underfill material is applied after solder reflow, filling the gap between the die and BT substrate. Fig. 8 shows a sample of the fabricated FCBGA package. Next, six FCBGA packages are mounted on a testing board, as shown on Fig. 9. Figures 10 and 11 illustrate the micrographs associated with the BGA and flip chip solder joint, respectively. As shown in Fig.11, the measured bump standoff height (59.45 μ m) and bump width (127.67 μ m) are close to the bump profile prediction results: bump standoff height (58.0 μ m) and bump width (129.7 μ m). This confirms the accuracy of the solder bump profile prediction. Once the FCBGA assembly is completed, the daisy chain network is also formed. With the daisy chain network, the measurements of the daisy chain electrical resistance can be accomplished during thermal cycle testing.

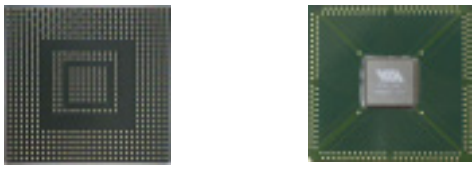


Fig.8: The flip chip BGA package

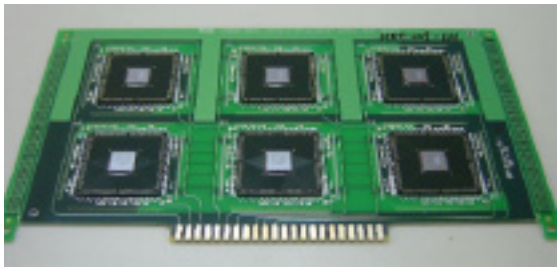
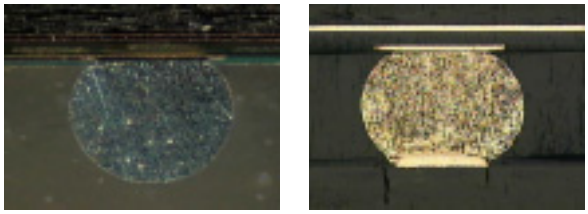


Fig.9: The flip chip BGA on a board



(a) (b)

Fig. 10: BGA solder ball, (a) before assembly, (b) after assembly

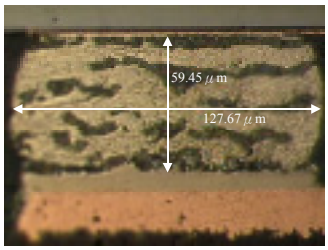


Fig. 11: Flip chip solder bump after assembly (MPE005-2L)

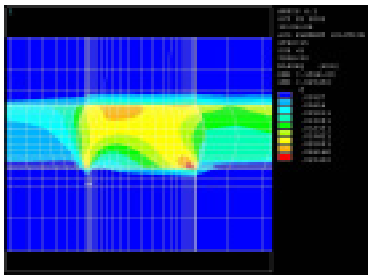
3.3 Testing set up

In order to distinguish the reliability of the five different flip chip packaging test vehicles, an ATC testing is employed in this investigation. Each of these designs comprises 24 FCBGA test samples. They are assembled to four testing boards (i.e., six packages per test board). JEDEC Condition-G is adopted to accomplish the test, in which it is composed of 6-minute linear temperature loading/unloading ramps, and 12-minute low/high temperature dwell periods, while the test temperature range is from -40 ^{o}C to 125 ^{o}C. The initial daisy chain resistance associated with these three FCBGA test designs is different owing to the variance in the designed structure and solder joint material. It is about 36 ohm to 39 ohm for MPE005-1H at room temperature, 34 ohm to 37 ohm for MPE006-1H, 33 ohm to 36 ohm for MPE007-1H, 37 ohm

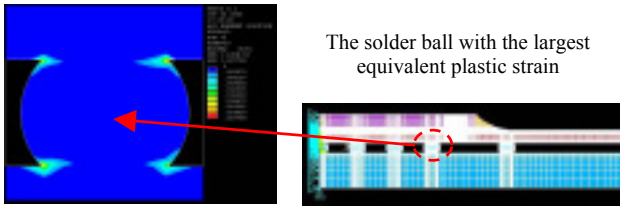
to 40 ohm for MPE005-1L and 30 ohm to 33 ohm for MPE005-2L.

4. RESULT AND DISCUSSION

4.1 FE analysis results



(a) The distribution of equivalent plastic strain on the solder joint



(b) The distribution of equivalent plastic strain on the BGA solder ball

Fig. 12: The distribution of equivalent plastic strain after five thermal cycles of package MPE006-1H

In the numerical ATC testing, the incremental equivalent plastic strain converges after about 5 thermal cycles. Based on the observation, the maximum accumulated equivalent plastic strain increment derived at the fifth temperature cycle will be employed for further evaluation of the fatigue life of the most critical solder joint. Fig. 12 shows the equivalent plastic strain distribution of MPE006-1H after five thermal cycles. It is found in Fig.12 (a) that the maximum equivalent plastic strain occurs in the pad-to-solder interface, near the BT substrate side at the outmost solder joint. Note that a similar result is also obtained in the other test vehicles. In Fig. 12(b), the maximum equivalent plastic strain on BGA solder balls takes place in the pad-to-solder interface near the BT substrate side, and the solder ball with the largest equivalent plastic strain is also indicated in this figure.

Simulation results of the FEM analysis of packages MPE005-1L, MPE005-2L, MPE005-1H, MPE006-1H and MPE007-1H are described as follows: package MPE005-1L has the maximum incremental equivalent plastic strain of 0.75% in the outermost solder bump. This strain is substituted into the Coffin-Manson equation (Eq.3) to obtain the mean cycle to failure at 6,439 cycles. The package MPE005-2L has the maximum incremental equivalent plastic strain of 0.73%. This strain is substituted into the Coffin-Manson equation to obtain the mean cycle to failure at 6,789 cycles. The maximum incremental equivalent plastic strain of package MPE005-1H is 0.72%. Its mean cycle to failure is 6,975 cycles. The maximum incremental equivalent plastic strain of package MPE006-1H is 0.67%. Its mean cycle to failure is 8,032 cycles. The maximum incremental equivalent plastic strain of package MPE007-1H is 0.65%. Its mean cycle to failure is 8,524 cycles.

At the same time, on the BGAs side, owing to the similar solder ball geometries and identical material, each model shows a similar maximum incremental equivalent plastic strain and mean cycle to failure, which are about 0.90% and 4,500 cycles, respectively. According to the simulation result, the flip chip solder joints show better reliability than the BGA solder balls.

4.2 ATC testing results

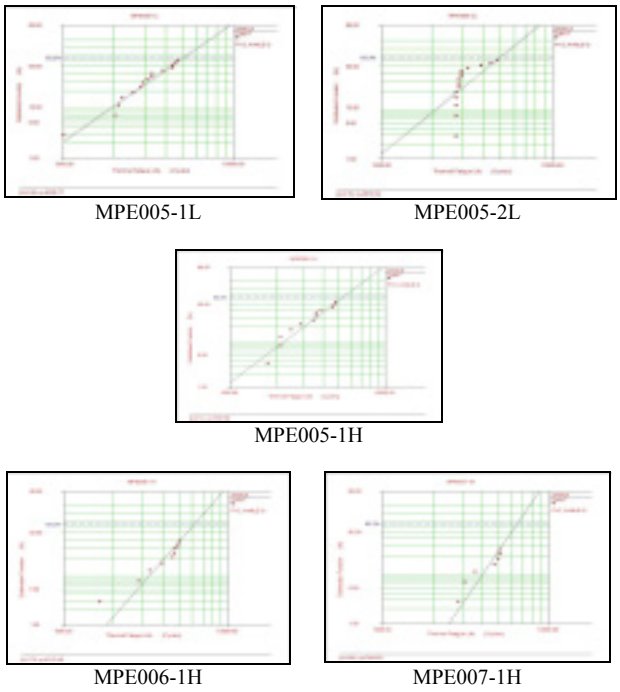


Fig.13: The Weibull distribution of the test vehicles

In the duration of ATC testing, the failure criteria of 10% upgrade of daisy chain electrical resistance is employed to define the solder joint fatigue. A Weibull distribution of the solder joint thermal fatigue life associated with MPE005-1L, MPE005-2L, MPE005-1H, MPE006-1H and MPE007-1H, respectively, is shown in Fig.13. As can be seen in these figures, the characteristic life, defined as 63.2% accumulative failure rate, is 5,029, 4,876, 5,341, 6,169 and 6,395, corresponding to MPE005-1L, MPE005-2L, MPE005-1H, MPE006-1H and MPE007-1H, respectively,

In addition, Fig.14 illustrates the Weibull distribution of the BGA thermal fatigue life of test vehicle MPE006-1H. Due to the equivalent BGA geometry and material, similar results are also obtained in the other test vehicles. It is shown in Fig.11 that the characteristic life of BGA, defined as 63.2% accumulative failure rate, is 3,845. Note that the solder joint of each test vehicles shows a better reliability than that of the BGA one.

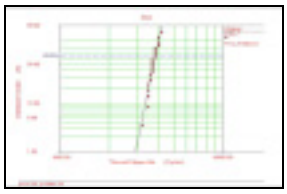


Fig.14: The Weibull distribution of the BGA

4.3 Comparison of experimental and FE results

The fatigue life of the BGA solder balls predicted by the FE modeling and experimental testing are 4,500 and 3,845, respectively. The fatigue life of the flip chip solder joints predicted by the FE modeling and experimental testing is illustrated in Fig.15. It is shown that the solution trend of these two approaches is in good agreement. Although some differences can be observed in the predicted fatigue life, the modeled results are still fair and satisfactory. Hence, the FE modeling can be claimed valid. The discrepancy might be due to the following implying factors: the 2-D plain strain FE modeling, the uncertainty of the experimental testing, the use of "equivalent" material properties for the BT substrate and FR-4 PWB, and the material properties assumed in the FE modeling etc.

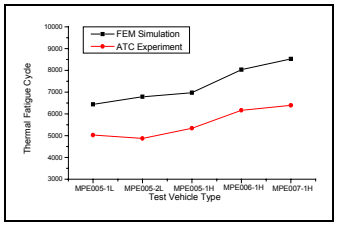


Fig.15: Comparison of the predicted fatigue life by experimental testing and FE modeling

4.3.1 For the effects of lead-free solder joint geometry on the solder joint reliability

Regardless of the modeled or the experimental results, MPE007-1H shows the best reliability, followed by MPE006-1H, and MPE005-1H. In other words, MPE005-1H presents the worst reliability. From a physical viewpoint, a solder joint with a larger solder volume and a higher standoff height can reduce the induced stress/strain. Based on the results, MPE007-1H would hold the best reliability among these three designs, owing to the fact that it consists of the largest solder volume and the highest standoff height. On the other hand, MPE005-1H has the smallest solder volume and the lowest standoff height among these three packages, and shows the worst reliability. It is worth noticing that, generally, a smaller contact angle can alleviate the stress/strain concentration effect of a solder bump. However, the contact angle plays a less significant part to the solder joint reliability than that of the standoff height in this study (since MPE007-1H shows the largest lower-contact-angle, followed by MPE006-1H and MPE005-1H). This is probably due to the fact that the underfill can alleviate the degree of stress concentration. It turns out that the effect of the contact angle in flip chip solder joint reliability is less significant as compared to that of the standoff height, when underfill is included in the package.

4.3.2 For solder joint reliability comparison between the 96.5Sn/3.5Ag lead-free and 63Sn/37Pb solders

The ATC result shows that the test vehicle of the flip chip package utilizing lead-free 96.5Sn/3.5Ag solder (MPE005-1L) shows a similar solder joint reliability to it utilizing the conventional 63Sn/37Pb (MPE005-2L) one. This confirms that the 96.5Sn/3.5Ag lead-free solder is a qualified bump material for flip chip applications.

4.4 Failure Analysis

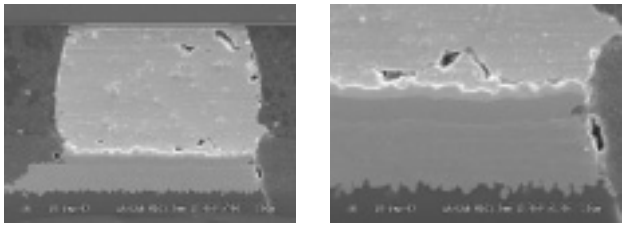


Fig. 16: A typical cross-sectional SEM graph of the fatigued solder joint

According to the specific layout design of the daisy chain, the location of the flip chip solder joint that is in fatigue failure can be identified through the measurement of the signals in the outmost solder joints during thermal cycle testing. According to the daisy chain measurement, the initial failed solder joint is located at the corner of the flip chip solder joint array. The fatigued solder joints in MPE005-1H, MPE006-1H, MPE007-1H, MPE005-1L, and MPE005-2L are cross-sectioned for failure analysis. Fig.16 illustrates a typical cross-sectional SEM graph of the fatigued solder joint, and a major fatigue crack is detected in the solder joint. In addition, the fatigue crack takes place in the pad-to-solder interface near the BT substrate side. The crack seems to initiate at the material and geometry singularity, and then propagates throughout the solder joint. This finding matches quite well with that of the FE modeling, as shown in Fig.12 (a), in which the maximum equivalent plastic strain also happened at the right-hand side of the lower pad, the same location as the crack initiation. The result again validates the FE modeling.

Moreover, the fatigued BGAs in the test vehicles are also cross-sectioned for failure analysis. Fig.17 depicts a typical cross-sectional micrograph of the fatigued BGA, and a major fatigue crack is observed in the BGA. In addition, the fatigue crack takes place in the pad-to-solder interface near the BT substrate side but the FR-4 testing PWB side. This result still matches well with that of the FE modeling.

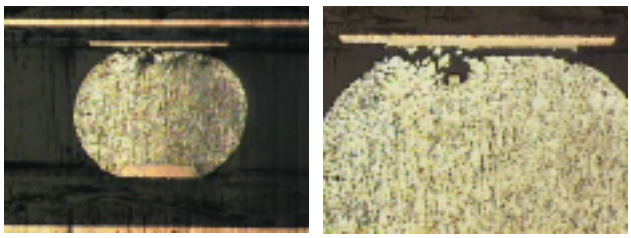


Fig. 17: A typical cross-sectional micrograph of the fatigued BGA

5. CONCLUSIONS

Through FE modeling and experimental validation by ATC testing, the dependence of the solder joint reliability of a fine-pitched flip chip BGA package on the solder geometry and solder material were extensively investigated. The geometry profile of the flip chip solder joints of the test vehicle, which is defined as MPE005-1H, MPE006-1H and MPE007-1H, was predicted using the forced-balanced method. More importantly, based on the predicted results, a simple design rule was created to readily assess the reliability performance of solder joints. It suggests that a larger solder volume with a higher standoff height could provide a better solder joint reliability. In terms of the effect of the solder material on the solder joint reliability of the test vehicles, which are defined as MPE005-1L and MPE005-2L, they were compared and consequently indicated that the test vehicle of the flip chip package utilizing lead-free 96.5Sn/3.5Ag solder shows a competed solder joint reliability to it utilizing the conventional 63Sn/37Pb one. In addition, both the experimental and the FEM results indicate that the solder joint of each test vehicles shows a better reliability than that of the BGA one.

From the failure analysis, it is also found that the FE modeling matches quite well with the experimental testing, in which the fatigue crack on the solder joint takes place in the pad-solder interface of the BT substrate side, and the fatigue crack on the BGAs takes place in the pad-solder interface of the BT substrate side. In addition, the location of the maximum equivalent plastic strain is consistent with that of the crack initiation.

6. ACKNOWLEDGEMENTS

The authors would like to thank the VIA Technology Corporation for providing the financial support for this research.

7. REFERENCES

1. Heinrich, S. M., Schaefer, M., Schroeder, S. A., and Lee, P. S., “Prediction of Solder Joint Geometries in Array-Type Interconnects”, ASME Journal of Electronic Packaging, Vol. 118, No. 3, September, 1996, pp. 114-121.

2. Chiang, K. N., and Chen, W. L., “Electronic Packaging Reflow Shape Prediction for the Solder Mask Defined Ball Grid Array”, ASME Journal of Electronic Packaging, Vol. 120, No.2, June, 1998, pp. 175-178.

3. Pfeifer, M. J., “Solder Bump Size and Shape Modeling and Experimental Validation”, IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 20, No. 4, November, 1997, pp. 452-457.

4. Liu, C. M., and Chiang, K. N., “Solder Shape Design and Thermal Stress/Strain Analysis of Flip Chip Packaging Using Hybrid Method”, Proc. 2000 Int’l Symp on Electronic Materials & Packaging, Hong Kong, November, 2000, pp. 44-50.

5. Chiang, K. N., Lin, Y. T., and Cheng, H. C., “On Enhancing Eutectic Solder Joint Reliability Using a Second-Reflow-Process Approach”, IEEE Transactions on Advanced Packaging, Vol. 23, No. 1, February, 2000, pp. 9-14.

6. Mercado, L.L., Sarihan, V., Guo, Y. F., and Mawer, A., “Impact of Solder Pad Size on Solder Joint Reliability in Flip Chip PBGA Packages”, IEEE Transactions on Advanced Packaging, Vol. 23, No.3, 2000, pp. 415-420.

7. Mercado, L. L., and Sarihan, V., “Predictive Design of Flip-Chip PBGA for High Reliability and Low Cost”, 49th Electronic Components and Technology Conference, San Diego, CA, USA, 1999, pp. 1111-1115.

8. Rosner, B., Liu, J., and Lai, Z., “Flip Chip Bonding Using Isotropically Conductive Adhesives”, Electronic Components and Technology Conference, 1996, pp. 578-581.

9. Zhenwei Hou, Guoyun Tian, Casey Hatcher, R. Wayne Johnson, Erin K. Yaeger, Mark M. Konarsai, and Lawrence Crane, “Lead-Free Solder Flip Chip-On-Laminate Assembly and Reliability”, IEEE Transactions on Electronics Packaging Manufacturing, Vol.24, No.4, October, 2001, pp. 282-292.

10. Charles Zhang, Jong-Kai Lin, and Li Li, “Thermal Fatigue Properties of Lead-Free Solders on Cu and NiP Under Bump Metallurgies”, Electronic Components and Technology Conference, 2001

11. Chiang, K. N., and Yuan, C. A., “An Overview of Solder Bump Shape Prediction Algorithms with Validations”, IEEE Transactions on Advanced Packaging, Vol. 24, No.2, May, 2001, pp. 158-162.

12. Solomon, H. D., “Fatigue of 60/40 Solder, ” IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-9, 1986, pp.91-104.