Parametric Design and Reliability Analysis of Wire Interconnect Technology Wafer Level Packaging

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The demands for electronic packages with lower profile, lighter weight, and higher input/output (I/O) density have led to rapid expansion in flip chip, chip scale package (CSP) and wafer level packaging (WLP) technologies. The urgent demand high I/O density and good reliability characteristics have led to the evolution of ultra high-density non-solder interconnection, such as wire interconnect technology (WIT). New technology, which uses copper posts to replace the solder bumps as interconnections, has improved reliability. Moreover, this type of wafer level package produces higher I/O density, as well as ultra fine pitch. This research focuses on the reliability analysis, material selection and structural design of WIT packaging. This research employs finite element method (FEM) to analyze the physical behavior of packaging structures under thermal cycling conditions to compare the reliability characteristics of conventional wafer level and WIT packages. Parametric studies of specific parameters will be performed, and the plastic and temperature-dependent material properties will be applied to all models.
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Keywords: Wafer Level Packaging, Chip Scale Package; Wire Interconnect Technology

Introduction

The function and design of IC tend to be complex. Packages are designed to decrease the interconnection pitch and use the area array types to increase the I/O counts. To solve the I/O limitations of conventional packaging technologies, flip chip and wafer level packaging technologies were formed. Wafer level packaging technology has the advantage of area array packages, such as ease of fabrication and reduced cost. However, wafer level packaging has some weaknesses, such as poor reliability and die size limitations. Hence, much research has focused on the reliability of flip chip and wafer level packages using finite element methods. Normally, the key factors, which influence a package's reliability are the geometry of the solder joint, underfill material, solder material, as well as its geometrical and structural configuration. Elenius [1] introduced the wafer level package, as well as the study of UltraCSP wafer level package, including the constructing of components, assembly and parametric reliability testing. To evaluate the reliability life of electronic packages, its failure modes must be addressed. Furthermore, the mechanical behavior of eutectic solder must be nonlinear as well as temperature-dependent to determine the actual physical behavior of a package. Wang et al. [2] studied the creep behavior of a flip chip package using hyperbolic power law to describe the creep behavior. In general, thermal cycling fatigue is a major failure modes of electronic packaging. Two reliability life prediction models have been adopted widely by electronic packaging researchers. Darveaux et al. [3] proposed a fatigue life model for solder joints using energy-density criterion. Instead of energy-density concept, many researchers used strain-based Coffin-Manson empirical formation [3,4] to predict solder life. Recently, much research has focused on the effect of plastic shear strain on reliability. However, according to the comparative study of flip chip in experimental data and computer simulation indicate that a flip chip package, where strain is not dominated by the shear strain, other strains, such as axial strain, should be considered for failure prediction. Conventionally, the wafer level package does not apply the underfill material to ensure the reliability of the solder joint, so the wafer level package must adopt an interface mechanism, such as a buffer layer, to reduce the mismatched stresses. However, many studies have shown that in the case of a large die size, such as 10 mm by 10 mm bare die, the conventional wafer level package does not meet the reliability requirements. The WIT wafer level package (Love et al. [5], Fig. 1) is more reliable than the conventional wafer level package. The geometry and material parametric analysis of the WIT wafer level package is examined herein to determine the reliability characteristics. Furthermore, the WIT reliability results are compared with conventional solder bump type wafer level packages. This study explores the alternative structure, which possesses higher I/O density and better interconnect reliability.

Methodology

The literature survey reveals that wafer level/flip chip packaging reliability is influenced significantly by the I/O connection type and material properties, such as solder ball type, column post type, Young's modulus and coefficient of thermal expansion (CTE). In this research, post size, material behavior and buffer layer geometry are the key design parameters of our parametric

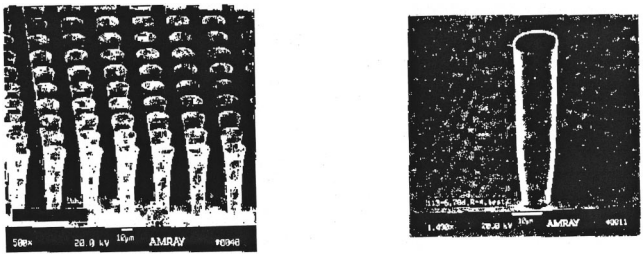

Fig. 1 Wire interconnect technology (source: Fujitsu)

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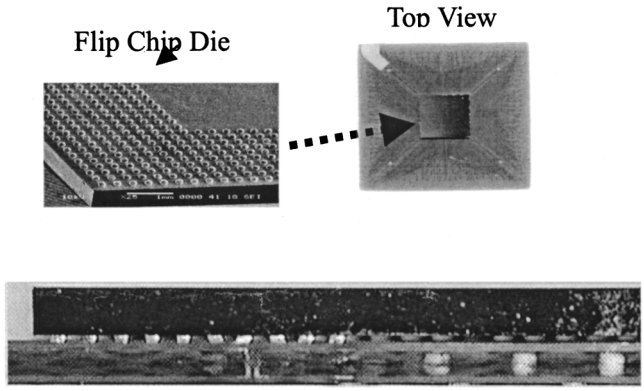

Fig. 2 Top and cross-section view of conventional flip-chip BGA package without underfill layer

Table 1 Material properties of baseline flip-chip BGA

	Young's modulus(Mpa)	Poisson ratio	CTE(ppm)
Silicon Chip	130,000	0.28	2.62
BT	19,000	0.2	15
Solder(60Sn/40Pb)	Nonlinear	0.35	25

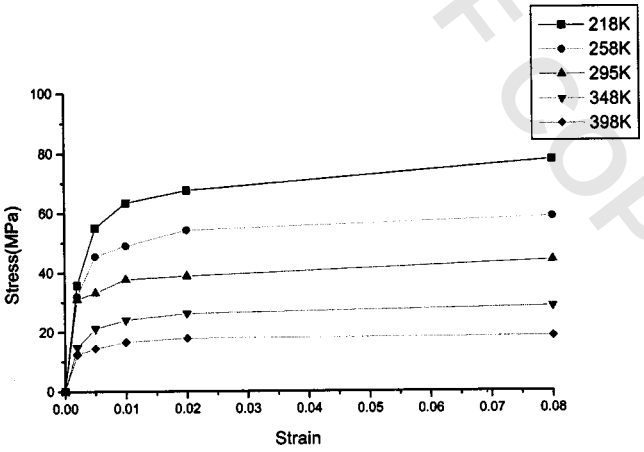

Fig. 3 Stress/strain curve of 60Sn/40Pb eutectic solder

study. Furthermore, herein, the multi-linear kinematic hardening rule was adopted as the stress-strain hysteresis option. The fatigue life of a eutectic solder joint can be predicted by using an empirical Coffin-Manson relationship (Coffin [6], Manson [7], and Sauber [8]).

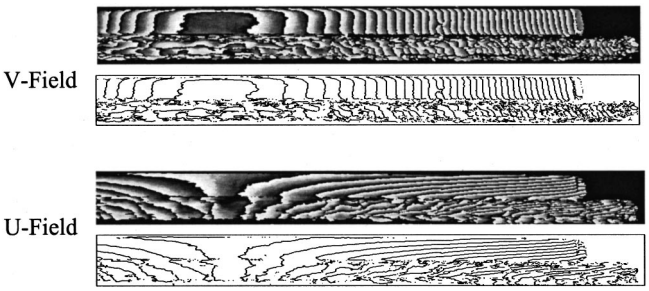

Fig. 5 Flip chip without underfill Laser Moiré phase diagram and refined fringe

$$N_f = C(\Delta\varepsilon_{eq})^{-n} \tag{1}$$

where N_f is the mean cycle to failure, C is the coefficient of fatigue ductility with a value of 0.4405 for solder ball type BGA and 0.001 for pin grid array, $\Delta\varepsilon_{eq}$ is the incremental equivalent plastic strain range in one cycle of thermal loading, and n is the fatigue ductility exponent, which is 1.96 for solder ball type BGA and 3.57 for pin grid array. Once the cyclic equivalent strain range of the solder is derived, the corresponding fatigue life can then be estimated. The accumulated and incremental equivalent plastic strain can be expressed as

$$\varepsilon_{eq}^{pl} = \sum \Delta\varepsilon_{eq}^{pl} \tag{2}$$

$$\Delta\varepsilon_{era}^{pl} = \frac{\sqrt{2}}{3}\left[(\Delta\varepsilon_x^{pl}-\Delta\varepsilon_y^{pl})^2+(\Delta\varepsilon_y^{pl}-\Delta\varepsilon_z^{pl})^2+(\Delta\varepsilon_z^{pl}-\Delta\varepsilon_x^{pl})^2 + \frac{3}{2}(\Delta\gamma_{xy}^{pl^2}+\Delta\gamma_{yz}^{pl^2}+\Delta\gamma_{xz}^{pl^2})\right]^{1/2} \tag{3}$$

where ε_{eqa}^{pl} is the accumulated equivalent plastic strain, and $\Delta\varepsilon_{eqa}^{pl}$ is the incremental equivalent plastic strain.

Validation Model

The simulation validation package considered herein is a conventional flip-chip BGA package without an underfill layer. Figure 2 shows the top view and center cross-sections of a conventional flip-chip BGA package. Notably, this validation package model is 37×37 mm square with 0.5 mm thickness of BT substrate and its die size is 11×11 mm, 0.5 mm thick and has ten rows of perimeter eutectic solder bumps. The standoff height of the eutectic solder joint is 0.131 mm with 0.2 mm ball pitch. Furthermore, Table 1 lists the elastic material properties of these components. Notably, the silicon die and BT materials are assumed to be linearly elastic and temperature independent. However, the thermoplasticity models for eutectic solder (40%Pb/60%Sn) materials (Fig. 3) were applied as an input of finite element thermal loading

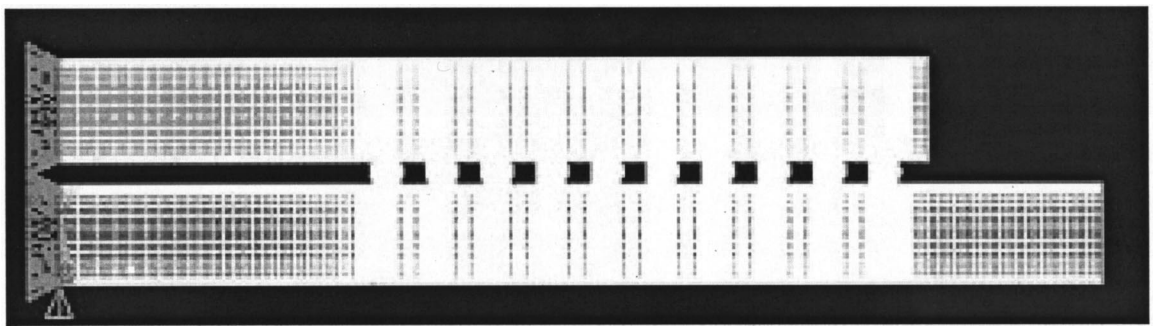

Fig. 4 One-half finite element model of flip-chip BGA package

Table 2 Simulation and experimental results of conventional WLP

Models	Finite element results		Experiment results	
	V-Field (μm)	U-Field (μm)	V-Field (μm)	U-Field (μm)
Conventional Flip-Chip BGA without underfill layer	16.6	3.6	15.3	4.17

analysis. Figure 4 illustrates a 2D flip chip finite element model without underfill material.

This conventional flip-chip BGA package was subjected to an external thermal loading condition, that is, from a 125°C stress-free condition the temperature was decreased to 25°C. Figure 5 presents the displacement of V-field and U-field laser moiré phase diagram as well as the refined fringe of the three cases. Table 2 shows the finite element simulation and experimental results. Clearly, via experimental measurements, the finite element approach demonstrates promising results for the validation model. Therefore, the finite element approach that was used in this research is a reliable method for the new WIT wafer level package design.

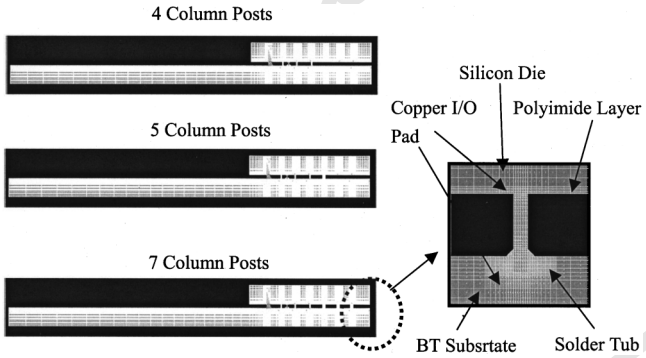

Fig. 6 Half FEM Model of WIT wafer level package with 4, 5 and 7 column posts

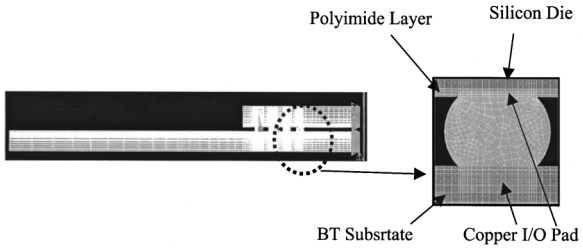

Fig. 7 Half FEM model of conventional wafer level package with 4 solder bumps

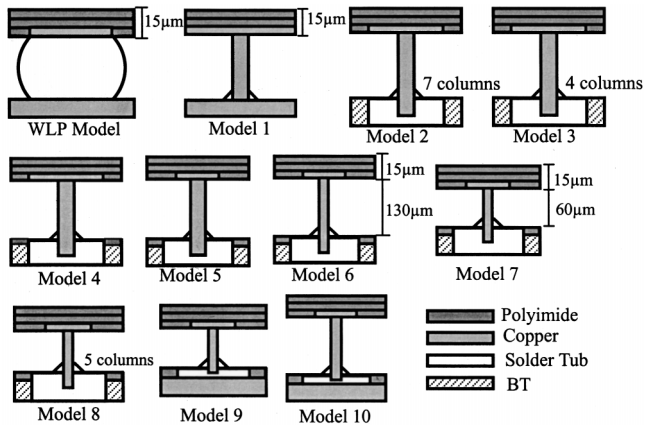

Fig. 8 Illustrations of FEM models of parametric study

Wire Interconnect Technology (WIT)

In studying the WIT mechanism, FEM analyses were performed on several parametric study models. Since the WIT package is designed to replace the conventional solder bump interconnect, for comparison, some WIT models p with the same I/O density as the conventional wafer level package were built. Moreover, the pitch and the original standoff height was also the same as the conventional solder bump model (60 μm and 130 μm, respectively), and 15 μm of polyimide layer was used as the die side buffer layer. Figure 6 shows the FEM model of WIT package with 4, 5, and 7 column posts on half of the package. Figure 7 illustrates a conventional wafer level package that contains 4 solder bumps on half of the package. In the model 1 (Fig. 8), seven copper columns were mounted directly, via eutectic solder around the copper post, to the copper I/O substrate pads. However, the model 2 has an alternate interconnection mechanism, which is a tub containing eutectic solder and a copper post inserted therein. In the third model, the number of the copper posts are reduced to four, with other configurations the same as the second model. Furthermore, the design of the substrate-side mechanism was altered from the previous models. In the fourth model, a 25 μm-thick polyimide layer was added to the substrate surface. In the fifth model, the diameter of the die-side pad was decreased to 115 μm. The copper posts were reduced from 30 μm to 20 μm in the sixth model with other configurations the same as the fifth model.

Table 3 Material properties of the FEM models

Material	Yung's modulous (GPa)	Poisson's ratio	CTE (ppm/°C)
Solder	Temperature dependent	0.35	23.9
Silicon	112.4	0.28	2.62
Copper	117	0.31	17
Polyimide	Temperature dependent	0.34	40
Elastomer	0.0655	0.41	95
BT	Temperature dependent	0.20	15
FR-4	18.2	0.19	16

Table 4 Temperature-dependent Young's modulus of BT

Temperature (K)	E (Gpa)
218	10.9
258	10.4
295	9.9
348	9.6
398	9.1

Table 5 Properties of plated copper

T (°C)	E (Gpa)	σ_y (Mpa)	σ_f (Mpa)	ε_f	α (ppm)
22	45.6	149.5	252.2	.118	17.0
125	44.6	144.7	215.7	.118	17.3
200	39.7	119.9	172.2	.113	18.4

Ref. Subbarayan, 1996

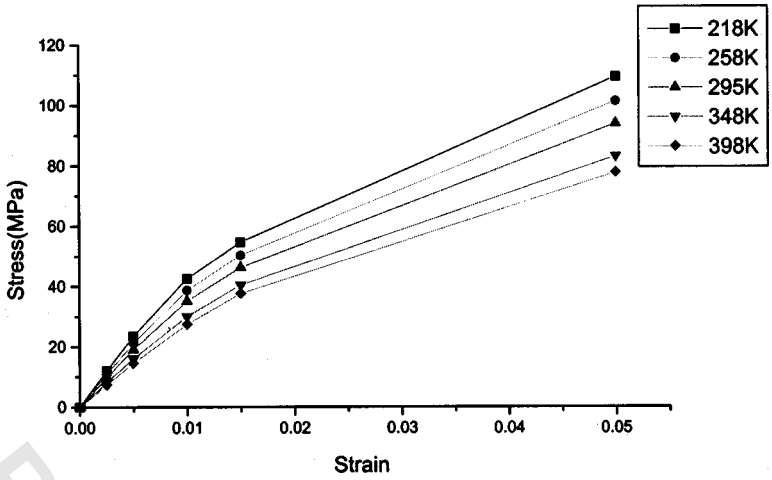

Fig. 9 Stress/strain curve of polyimide

The standoff height of the copper post was reduced from 130 μm to 60 μm in the seventh model. Finally, with the same configuration as in the seventh model, the eighth model adds one more copper post near the edge of the outer post, this post is served as a dummy post to increase the reliability. To examine the effect of solder tub depth, two more models (model 9 and 10) with solder tub of 25 μm depth and 60 μm with 5 columns and 130 μm with 4 columns, standoff height with solder tub of 25 μm depth were constructed.

Finite-Volumn-Weighted Averaging Technique

The stress/strain information near the interfaces of the solder joint and the silicon die and that of the solder joint and the PCB is effectively characterized. Note that the interfaces of these components usually involve an abrupt geometry change that inevitably forms a sharp corner and more importantly, induces a singular (concentrated) stress/strain response. Since the material nonlinearity is considered such that the stress concentration can be eventually eased, techniques that can be applied to characterization of the strain response around the singular point are in critical demand.

The plastic strain in the strain concentration area is very sensitive to the local mesh density, to avoid the mesh sensitivity an improved volume-weighted averaging technique is applied to effectively characterize the strain response in the corner of the solder joint. A specific zone is introduced and applied to perform the averaging technique as follows:

$$\tilde{\varepsilon} = \sum_{e=1}^{n_0} \int_{\Omega_e} \varepsilon_e d\Omega \Big/ \sum_{e=1}^{n_0} \int_{\Omega_e} d\Omega \tag{4}$$

where n_0 is the total number of elements in the zone, ε_e the strain of the e-th element, Ω_e the volume (area) of the e-th element, and $\tilde{\varepsilon}$ the volume-weighted averaging strain in a specific zone. The dimension of the finite zone is determined in an empirical manner. It should be small enough to capture the maximal strain field; on the other hand, large enough to obtain a converging solution as the mesh density increases.

Finite Element Analysis

The finite element models employed herein simulate the accelerated thermal cycling (ATC), as well as temperature rising and dwelling between −55°C and 125°C with a one-hour cycling rate, ramp-up, dwelling and ramp-down time are all 15 minutes. To ensure nonlinear convergency, a true Newton Raphson method with sub-step iteration was applied as the nonlinear iterative solution. Based on the specific sub-loading steps, the strain/stress results, which plot the hysteresis loop, were attained easily. Notably, the creep phenomenon and heat transfer were not included herein. Therefore, a steady-state condition is assumed.

Tables 3 and 4 present the material properties of all components, such as Young's modulus, Poisson's ratio, and CTE. Furthermore, critical materials, such as the eutectic solder (40Pb/60Sn), plated copper and the polyimide, employed herein are multi-linear and temperature dependent. Figures 3, 9, and Table 5

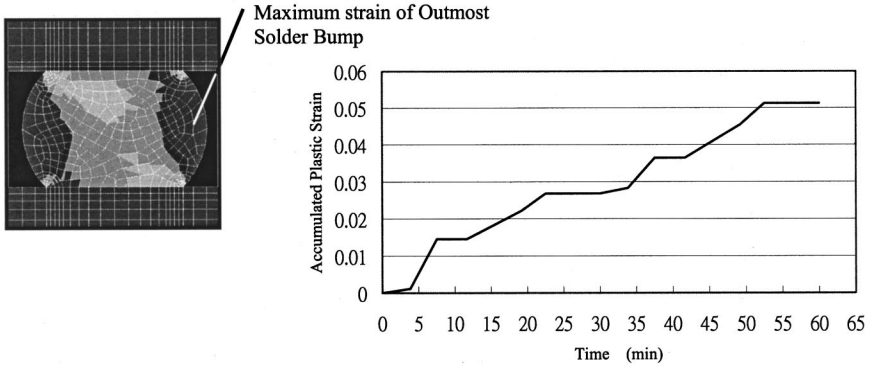

Fig. 10 Accumulated equivalent plastic strain versus cycling time of conventional WLP

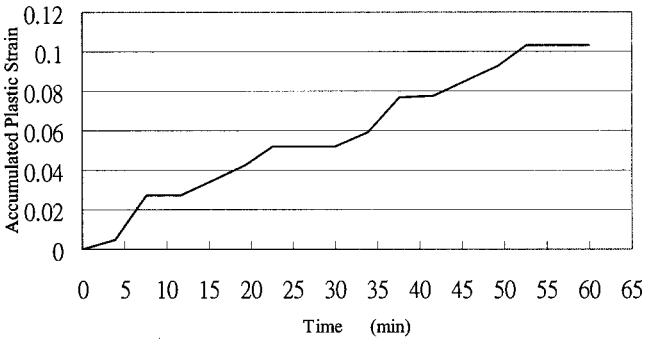

Fig. 11 Accumulated equivalent plastic strain versus cycling time of WIT Model 1

illustrate the stress-strain curves of these three materials. Simulation results of the FEM parametric study of the WIT package and conventional wafer level package are described below. The conventional wafer level package FEM model with four solder bump interconnections had the maximum one cycle accumulated equivalent plastic strain of 2.68% (Fig. 10) in the outermost bump. This strain was substituted into Coffin-Manson equation (C equal to 0.4405 and n equal to 1.96) to obtain the mean cycle to a failure of 530 cycles. In the first WIT package (Model 1, with 7 copper posts) prototype, the equivalent plastic strain of the outermost column is 5.19% (Fig. 11), and the mean cycles to failure for Coffin-Manson criterion (C equal to 0.001 and n equal to 3.57) is 39 cycles. A comparison of WIT and conventional WLP models reveals that the WIT model with copper posts mounted directly on the I/O pads was unacceptable. Thus, to improve the excessive strain of WIT Model 1, a solder tub structure (50 μm depth) on the copper I/O pad was adopted in the second model (Fig. 8, WIT Model 2). In this model, the maximum equivalent plastic strain, located in the solder of the solder tub (Fig. 12) had a value of 1.82%, which is equivalent to 1628 cycles. This result displays a dramatic improvement in the reliability life and yields results that are superior to the conventional wafer level package.

To further study the I/O number effect, the number of copper posts in the third model was reduced from seven to four (I/O numbers equal to the conventional WLP). The maximum equivalent plastic strain in the solder was increased to 1.91%, (1370 cycles), which is also much lower than that of the conventional solder bump. Furthermore, to consider the substrate configuration, a layer of polymimde (25 μm thickness) was added to cover part of the copper pad (solder mask defined) on the substrate in the fourth model (WIT Model 4). FEM simulation result shows that the maximum equivalent plastic strain increased to 2.05%, (1064 cycles). This was due to the stiffness of the polyimide, which is higher than both the eutectic solder and BT, if the strain is higher than a certain value. Subsequently, the I/O pad diameter on the die side decreased from 150 μm to 115 μm (WIT Model 5), the maximum equivalent plastic strain (for Model 5) is 2.06%, (1064 cycles), which almost the same as previous model. Furthermore, although other configurations were the same as in Model 5, the copper post diameter was reduced from 30 μm to 20 μm (WIT, Model 6). Analysis indicates that the maximum equivalent plastic strain for this model decreased to 2.03%, (1102 cycles). Since the thinner copper post provides more flexibility, the strain of the solder decreased as the diameter of the post are decreased, simultaneously. Furthermore, the standoff height of the copper posts was reduced to 60 μm for WIT Model 7, and became the design parameter. Notably, after thermal cycling, the equivalent plastic strain was increased to 4.09%, (90 cycles). Results show that the reliability of this model was poor. Therefore, the improvement methodology must be developed.

Thus, in the eighth model, the additional dummy interconnection was positioned next to the outermost I/O of the seventh model. The dummy I/O (WIT Model 8, Fig. 6 with 5 column posts) was designed to absorb the strain caused by thermal mismatch in the package. The equivalent plastic strain was reduced from 4.09% (90 cycles) to 2.5% (524 cycles). Finally, regarding the effect solder tub depth, its depth was reduced herein from 40 μm to 25 μm. Notably, models 9 and 10 contain 5 and 4 column posts with a 25 μm buffer layer on the substrate, 115 μm-diameter copper pads on the die side and have standoff heights of 60 μm and 130 μm, individually. The results of these models reveal that their equivalent plastic strains were 3.53% (153 cycles) and 2.16% (883 cycles), respectively. Clearly, compared with the previous models the depth of the solder tub influences the strain significantly. That is, a reduction in solder tub depth from 40 μm to 25 μm resulted in a strain increase from 2.5%/524 cycles to 3.53%/153 cycles (models 8 and 9), and from 2.12%/944 cycles to 2.16%/883 cycles (Model 6 and 10). Thus, solder tub depth could also be considered as an important design factor.

Conclusions

The parametric study of WIT herein revealed the impact of specific design parameters. To develop an optimal design, which solves the reliability issue, this research selected the dimensions and layout of copper post and solder tub as the design parameters. Moreover, for comparison purposes, the basic dimensions of the model were identical with that of the conventional wafer level package. From the analysis, the following conclusions were drawn:

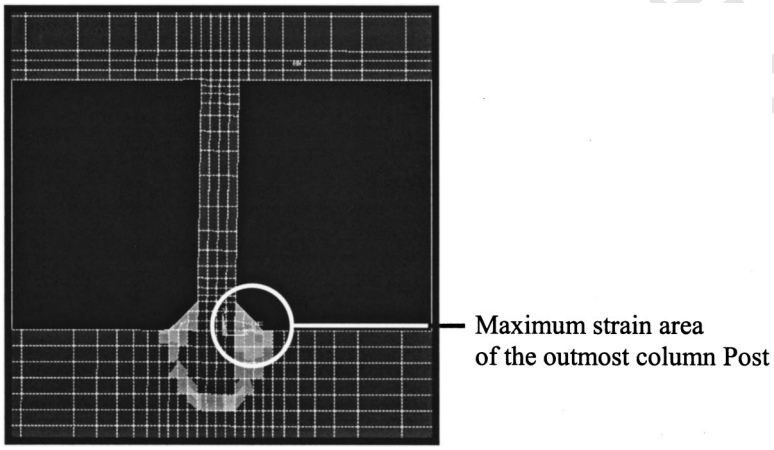

Fig. 12 Max. strain of outmost column post of WIT Model 2

Table 6 Results of FEM analysis of WIT package

Model	Incremental equivalent plastic strain (%)	No. of cycles
Conventional WLP model	2.68	530
Model 1	5.19	39
Model 2	1.82	1628
Model 3	1.91	1370
Model 4	2.05	1064
Model 5	2.06	1064
Model 6	2.03	1102
Model 7	4.09	90
Model 8	2.5	524
Model 9	3.53	153
Model 10	2.16	883

1. The design of copper posts mounted directly on the copper pads result in an excessive range of equivalent plastic strain for the solder adhesion. This design is not competitive with the conventional solder bump interconnect technology.
2. The solder tub design reduced the maximum strain of the solder interconnects effectively. That is, the copper posts inserted into the solder tub decreased the equivalent plastic strain, and results prove that a deeper tub depth provides better reliability life for the interconnect.
3. The diameter of the copper post affected the strain of the solder since reducing the diameter of copper post could ease the column-induced bending on the solder. When the diameter of I/O post was reduced from 30 μm to 20 μm, the equivalent plastic strain decreased from 2.06% (1064 cycles) to 2.03% (1102 cycles).
4. The equivalent plastic strain increased as the standoff height decreased.
5. An additional dummy I/O post could enhance the reliability life of the solder, effectively. WIT has the advantage of small pitch and high density, the strain of the solder will be reduced as the number of I/O increases.
6. With the same I/O number and standoff height the WIT shows a better reliability life than the conventional WLP.

Table 6 summarizes the reliability effect of each parameter. To conclude, the WIT presented herein has considerable potential in wafer level packaging applications.

Acknowledgments

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