

Parametric Reliability Analysis of No-Underfill Flip Chip Package

Kuo-Ning Chiang, Zheng-Nan Liu, and Chih-Tang Peng

Abstract—This research proposes a parametric analysis for a flip chip package with a constraint-layer structure. Previous research has shown that flip-chip type packages with organic substrates require underfill for achieving adequate reliability life. Although underfill encapsulant is needed to improve the reliability of flip chip solder joint interconnects, it will also increase the difficulty of reworkability, increase the packaging cost and decrease the manufacturing throughput. This research is based on the fact that if the thermal mismatch between the silicon die and the organic substrate could be minimized, then the reliability of the solder joint could be accordingly enhanced. This research proposes a structure using a ceramic-like material with CTE close to silicon, mounted on the backside of the substrate to constrain the thermal expansion of the organic substrate. The ceramic-like material could reduce the thermal mismatch between silicon die and substrate, thereby enhancing the reliability life of the solder joint. Furthermore, in order to achieve better reliability design of this flip chip package, a parametric analysis using finite element analysis is performed for package design. The design parameters of the flip chip package include die size, substrate size/material, and constraint-layer size/material, etc. The results show that this constraint-layer structure could make the solder joints of the package achieve the same range of reliability as the conventional underfill material. More importantly, the flip chip package without underfill material could easily solve the reworkability problem, enhance the thermal dissipation capability and also improve the manufacturing throughput.

Index Terms—Ceramic-like, constraint layer, CTE, flip chip, parametric analysis, reliability, reworkability, underfill.

I. INTRODUCTION

FLIP chip and wafer level packaging technologies currently attract increasing attention from the electronics packaging industry due to their good thermal performance, smaller size, lower profile, lighter weight, higher I/O density, etc. Conventionally, flip chip packages used an underfill encapsulant to reduce the strain of the solder joints between the IC chip and its substrate. This encapsulant not only provides dramatic reliability enhancement with minimal impact on the flip chip manufacturing process flow, but also extends to a variety of organic substrate materials, resulting a ten to hundred-fold improvement in reliability compared to a flip chip package without underfilling. However, the major shortcoming posed by the un-

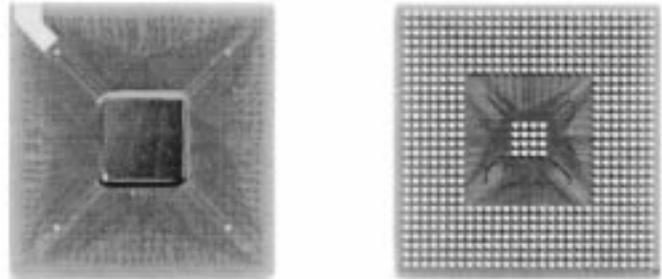


Fig. 1. Flip chip BGA.

derfilling process remains unresolved, such as, significantly increased difficulty of reworkability and the decrease of manufacturing throughput. To solve these problems, the main goal of this research is to develop an improved flip-chip package by eliminating the underfill material. This new packaging structure could not only maintain high reliability and low cost as the conventional flip chip packages but also could provide high process throughput, better thermal performance and high reworkability characteristics.

There has been substantial research on the flip chip package with underfill material for the past years. The influence of soldering and encapsulant processing conditions and materials on the reliability of flip chip on board structure is discussed by Giesler *et al.* [1]. The impact of under-filler particles on reliability of flip-chip interconnects has been discussed by Darha *et al.* [2]. They conducted parametric analytical studies to investigate whether the reliability of flip-chip interconnects is affected by inhomogeneities in the underfill, such as the setting of filler particles. The effect of underfill on the level of stress concentration is investigated by Madenci *et al.* [5]. They identified the possible failure sites of a flip chip package by using a global/local finite element approach. Furthermore, a no-flow underfill for low-cost flip-chip package has been developed by the Georgia Institute of Technology [4]. This new assembly technology is more cost-effective due to simplification of the process; however, the difficulty of reworkability and the reduction of manufacturing throughput are not yet fully resolved. All of these researches have shown that in order to maintain good reliability of solder joints, the underfill is a necessary structure for conventional flip chip packages.

This work studies a flip chip package using a CTE constrained material on the backside of the substrate instead of using a conventional underfill process. The results of finite element analysis show that this new flip chip package with an adequate structural configuration could significantly improve

Manuscript received September 1, 2000; revised May 1, 2001. This paper was recommended for publication by Associate Editor I. C. Ume upon evaluation of the reviewers' comments. This work was supported by the National Science Council under Project NSC 90-2212-E-007-014.

The authors are with the Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan 30055 R.O.C. (e-mail: knchiang@pme.nthu.edu.tw).

Publisher Item Identifier S 1521-3331(01)09776-8.

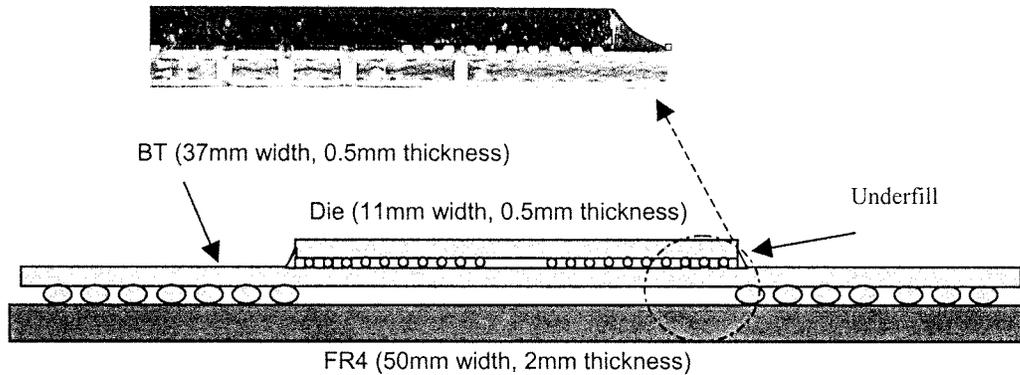


Fig. 2. Cross section of conventional flip chip BGA package.

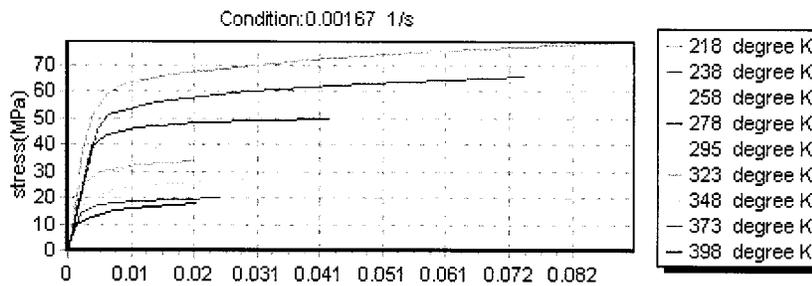


Fig. 3. Temperature dependent stress/strain curve of eutectic solder.

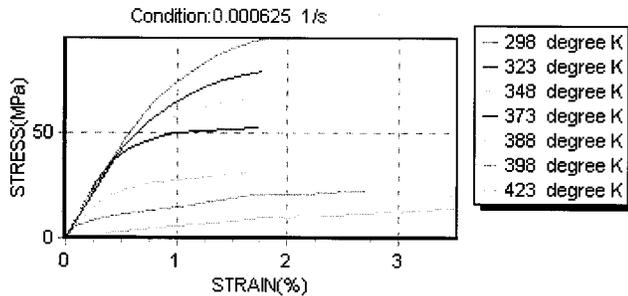


Fig. 4. Temperature dependent stress/strain curve of underfill material.

reworkability, increase manufacturing throughput, and enhance thermal performance, while still maintaining the same package reliability life as the underfilled flip chip structure.

Finite element analysis has been generally accepted by the electronics packaging research communities. Many structural/material behaviors of electronic packages are material/geometrically nonlinear, thermally dependent, strain rate dependent, time dependent (creep/relaxation) and even size, layout and process dependent. Therefore it is unlikely to set all of the nonlinear material properties as inputs for finite element analysis. Thus, one needs to carefully examine the analysis methodologies, procedures, mechanics/numerical algorithm selection, geometry configuration, boundary conditions and loading condition, etc. Usually, parametric analysis with 2D/3D finite element nonlinear analysis is quite feasible for electronic package analysis/design, and it has been widely adopted in the literature by [2], [3], [6], [8]–[10]. Thus this research will not focus on the prediction of reliability of the package but will

TABLE I
MATERIAL PROPERTIES OF TEST FLIP-CHIP BGA

	Young's Modulus(Mpa)	Poisson Ratio	CTE(ppm)
Silicon Chip	130,000	0.28	2.62
BT	19,000	0.2	15
Constraint Layer	130,000	0.28	2.62
Copper Pad	117,000	0.31	17
Solder Mask	3,448	0.35	30
FR-4	18,200	0.19	16
Solder(60Sn/40Pb)	Nonlinear	0.35	25

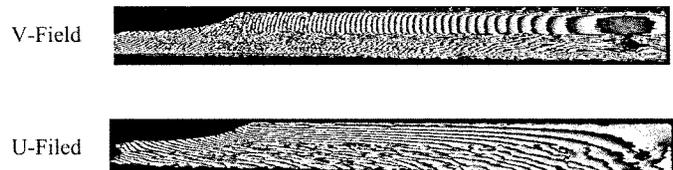


Fig. 5. Conventional flip chip laser Moire' phase diagram.

use parametric analysis technology to compare the impact of the strain and reliability characteristics on both the new and the conventional flip chip packages under same thermal loading condition. The results should be useful for the design of the new no-underfill flip chip package.

II. FLIP CHIP TEST STRUCTURES FOR VALIDATION

In order to validate the finite element approach applied in this research, a conventional flip chip BGA package (Fig. 1) is selected as a test vehicle in this study. The package is mounted on a multilayer FR-4 printed wiring board (PWB). On the BGA side,

TABLE II
SIMULATION AND EXPERIMENTAL RESULTS

Test Model	Finite Element Results		Experiment Results	
	V-Field (μm)	U-Field(μm)	V-Field (μm)	U-Field(μm)
Flip Chip with Underfill	22.9	4.5	22.5	3.75

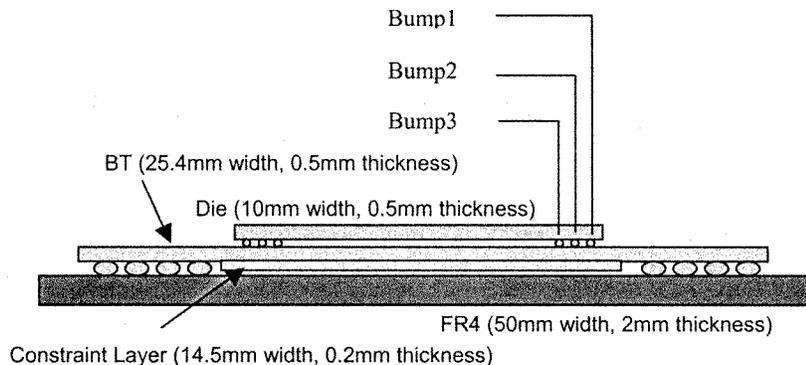


Fig. 6. Flip chip BGA package with constraint layer.

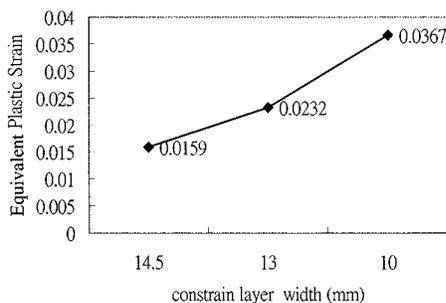


Fig. 7. Constraint layer width versus equivalent plastic strain.

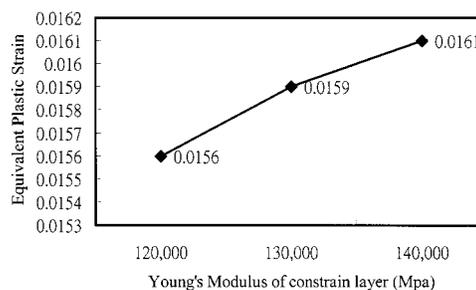


Fig. 8. Young's modulus of constraint layer versus equivalent plastic strain.

it contains seven rows of perimeter eutectic solder joints with 1.27 mm ball pitch and 0.508 mm standoff height. Center cross-sections of a conventional flip-chip BGA package are shown in Fig. 2. The dimension of the package is 37 × 37 mm square with a BT substrate thickness of 0.5 mm; the package die size is 11 × 11 mm with a thickness of 0.5 mm; and the standoff height of the eutectic solder joint of the flip chip is 0.131 mm with 0.2 mm ball pitch. The elastic material properties of these components within the package are listed in Table I. It should be noted that the silicon die, BT, copper pad, solder mask, constraint layer and FR-4 materials within the package are assumed to be linearly elastic and temperature independent. However, the non-linear thermo-plasticity models are applied for eutectic solder (40%Pb/60%Sn, Fig. 3) and the underfill material (Fig. 4) in the nonlinear finite element thermal stress/strain analysis [11].

The packaging model was subjected to external thermal loading, dropping from an initial stress free condition, i.e., 125 °C, to a room temperature 25 °C. The V-field (vertical direction) and U-field (horizontal direction) displacement phase diagrams of laser moiré for these practices are shown in Fig. 5, and the finite element simulation and experimental results are listed in Table II. It can be seen that the finite element approach demonstrates promising results in comparison with the measurements. Therefore, the finite element approach used in this research can be considered as a reliable method for the subsequent new package design.

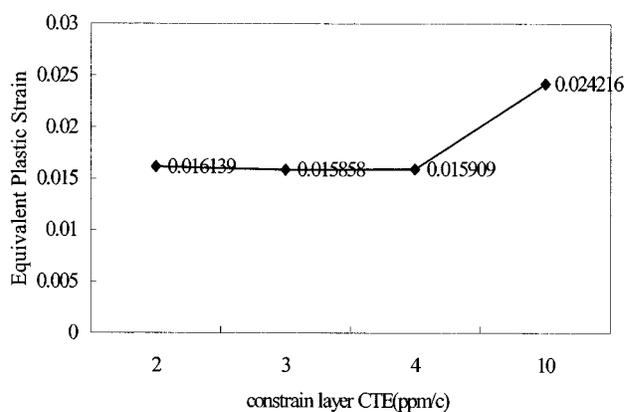


Fig. 9. CTE of constraint layer versus equivalent plastic strain.

III. FATIGUE LIFE PREDICTION MODEL

The fatigue life of a eutectic solder joint can be predicted using an empirical Coffin–Manson relationship [7], [8], [12]–[14]

$$N_f = \frac{1}{2} \left(\frac{\Delta \epsilon_{eq}^{pl}}{2 \epsilon_f} \right)^{(1/c)} \tag{1}$$

$$N_f = 0.4405 \cdot (\Delta \epsilon_{eq}^{pl})^{-1.96} \tag{2}$$

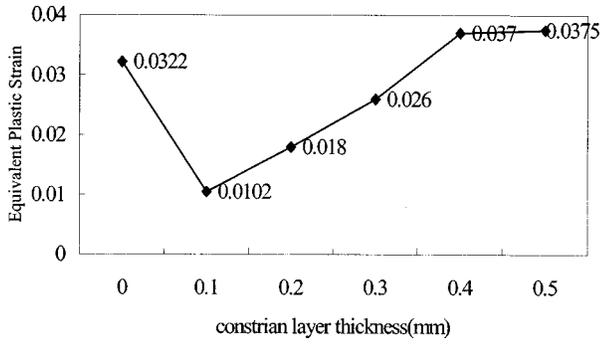


Fig. 10. Thickness of constraint layer versus equivalent plastic strain.

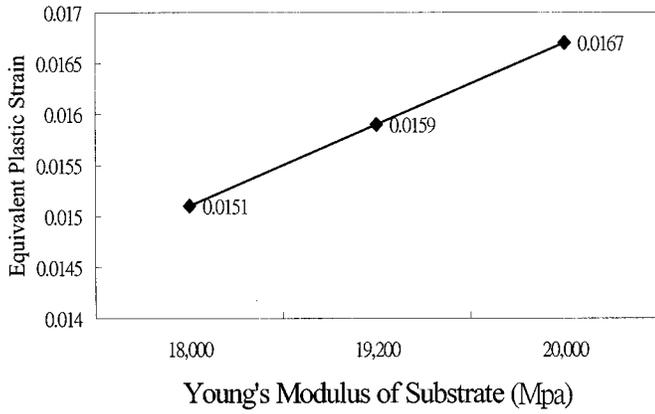


Fig. 11. Young's modulus of substrate versus equivalent plastic strain.

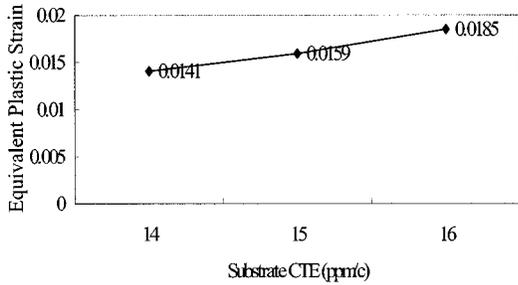


Fig. 12. Substrate CTE versus equivalent plastic strain.

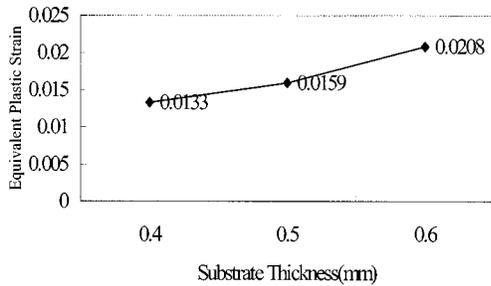


Fig. 13. Substrate thickness versus equivalent plastic strain.

where

- N_f mean cycle to failure;
- $\Delta\epsilon^{IE}$ equivalent plastic strain range in one cycle of thermal loading;
- ϵ_f fatigue ductility coefficient;
- c fatigue ductility exponent.

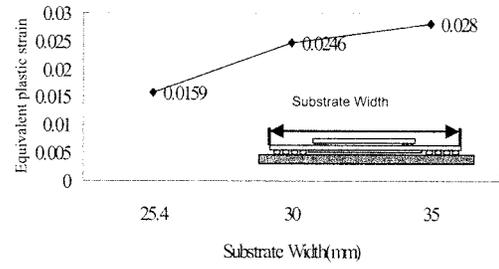


Fig. 14. Substrate width versus equivalent plastic strain.

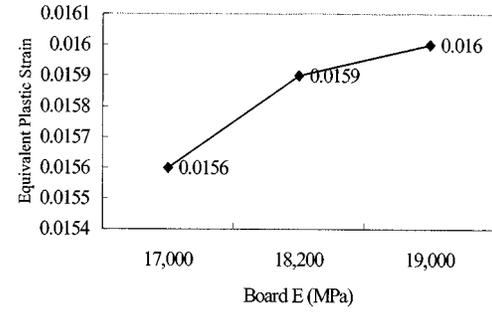


Fig. 15. Young's modulus of PWB versus equivalent plastic strain.

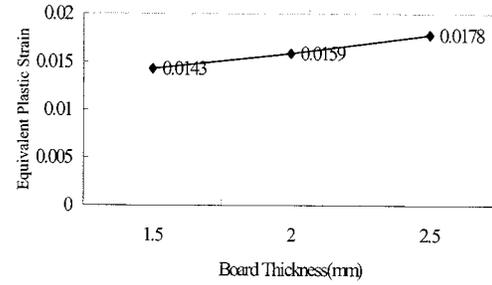


Fig. 16. Thickness PWB versus equivalent plastic strain.

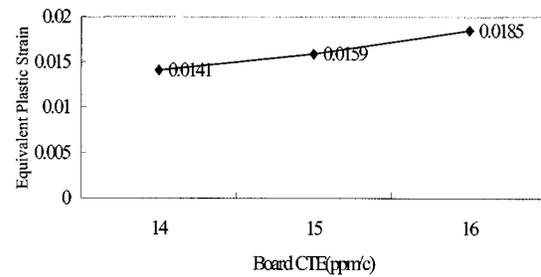


Fig. 17. CTE of PWB versus equivalent plastic strain.

This exponent is generally between -0.5 and -0.7 , and in this study is assumed to be -0.51 . Thus equation (1) can be re-written as equation (2). The accumulated effective plastic strain is defined by

$$\epsilon_{eq}^{pl} = \sum_{i=1}^n \Delta\epsilon_{eq}^{pl} \quad (3)$$

$$\Delta\epsilon_{eq}^{pl} = \frac{\sqrt{2}}{3} \left[(\Delta\epsilon_x^{pl} - \Delta\epsilon_y^{pl})^2 + (\Delta\epsilon_y^{pl} - \Delta\epsilon_z^{pl})^2 + (\Delta\epsilon_z^{pl} - \Delta\epsilon_x^{pl})^2 + \frac{3}{2} (\Delta\gamma_{xy}^{pl^2} + \Delta\gamma_{yz}^{pl^2} + \Delta\gamma_{xz}^{pl^2}) \right]^{1/2} \quad (4)$$

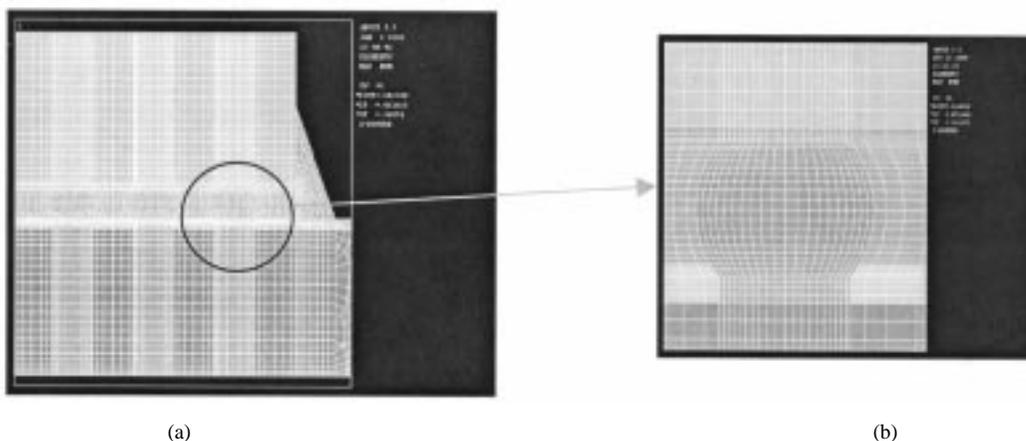


Fig. 18. Two-dimensional finite element model for conventional flip chip package.

TABLE III
DESIGN PARAMETERS VERSUS RELIABILITY

	Constraint Layer		PWB Thickness	Substrate	
	Thickness	Width		Width	Thickness
Dimension	See Figure 10	Up	Up	Up	Up
Reliability Life	See Figure 10	Up	Down	Down	Down

	Substrate		PWB		Constraint Layer CTE
	E	CTE	E	CTE	
Material Property	Up	Up	Up	Up	Up
Reliability Life	Down	Down	Down	Down	Down

where

- ϵ_{eq}^p accumulated effective plastic strain;
- i load step;
- ϵ_m^p normal component of plastic stress parallel to m axis;
- γ_{mn}^p plastic shear component.

Once the cyclic equivalent plastic strain range of the solder joint is obtained, the corresponding fatigue life can then be estimated.

IV. PARAMETRIC STUDY OF NEW FLIP CHIP PACKAGE

The objectives of this research were to address some of the reliability issues in flip chip packages by means of characterizing the plastic equivalent strain responses of flip chip package structures under various configurations. Parametric studies were performed to investigate the effects of die size, substrate size and its material properties, PWB size and its material properties and the size/material properties of the backside CTE constraint layer of the flip chip package. In the parametric study, the solder ball layout of the new flip chip die is a 3×3 area array peripheral type, and the other configurations of the package are shown in Fig. 6. The thermal cycling temperature was from -55 °C to 125 °C with a 1-h thermal cycling rate. The key parameters investigated in this study include the width, thickness, CTE and Young’s modulus effect of the die, substrate, PWB, buffer layer and the constraint layer of the packages.

A. Constraint Layer Effects

As shown in Fig. 7, an increase of the width of the constraint layer from 10 mm to 14.5 mm can significantly decrease the average equivalent plastic strain of the flip chip solder ball from 0.0367 to 0.0159. From equation (2), it is easy to see that the

reliability life of the solder ball will increase from 286 cycles to 1476 cycles. The constraint layer length of 14.5 mm is selected as the maximum width that can be used for this particular package, and in this case all of the equivalent plastic strains occur at solder bump 1 (Fig. 6). The Young’s modulus effect of the constraint layer is shown in Fig. 8, indicating that the effect of the Young’s modulus within the range of 120 Gpa to 140 Gpa on the equivalent strain is insignificant. Fig. 9 shows the CTE effect of the constraint layer. It presents that the equivalent strain will increase as the CTE difference between the silicon die and the constraint layer increases. Furthermore, for the thickness effect of the constraint layer, Fig. 10 indicates that with a constraint layer thickness of around 0.1 mm there are the minimum equivalent plastic strain (1.02%) and the maximum reliability life (3330 cycles) for the new package.

B. Substrate Size and Material Properties Effects

The substrate design parameters include material properties and geometrical configurations such as the Young’s modulus, CTE, thickness and width. The equivalent plastic strain versus each design parameter is shown in Figs. 11–14. The figures indicate that the equivalent plastic strain increases as the Young’s modulus, CTE, thickness and width increase. It is clear that an easier way to reduce the equivalent plastic strain of the solder bump is to use a thinner or a flexible/compliant substrate.

C. PWB Size and Material Properties Effects

The design parameters considered in the PWB include material properties and geometrical configurations, such as the Young’s modulus, CTE and thickness. The results of equivalent

plastic strain versus each design parameter are shown in Figs. 15–17. The figures indicate that the equivalent plastic strain increases as the Young's modulus, CTE, and thickness increase.

D. Analysis of Conventional Flip Chip Package

For comparison purpose, the thermal stress/strain behavior of a conventional flip chip package (with an underfill structure and without a constraint layer) is studied in this research, using the same structural configurations, such as die size, bump size/layout, and substrate size the same as Fig. 6. The underfill material property is shown in Fig. 4. A 2-D mesh for the finite element analysis is shown in Fig. 18(a) and the fringe curve of the equivalent plastic strain at 125 °C is shown in Fig. 18(b). From Fig. 18(b) it can be seen that the maximum equivalent plastic strain is located in the right upper corner of the outermost solder bump. The equivalent plastic strain ($\Delta\epsilon_p$) under thermal cycling (–55 °C to 125 °C) for this particular solder bump is 0.009 13, and the reliability life obtained from equation (2) is 4215 cycles. In the case of the conventional flip chip package without underfill structure, the equivalent plastic strain ($\Delta\epsilon_p$) increases to 0.0313 and the reliability life significantly decreases to 391 cycles. These results indicate that the underfill is a necessary structure to increase reliability life for the conventional flip chip package.

To conclude, a parametric study using finite element analysis has been performed over number of design parameters including the die size, substrate size and its material properties, PWB size and its material properties and the size/material properties of the backside CTE constrain layer of the flip chip package. The effects of each design parameter are shown in Table III, and it could be a guideline for the new flip chip package design.

V. CONCLUSION

This research proposed a flip chip package using a CTE constraint layer mounted on the backside of a substrate to confine the thermal expansion of the organic substrate. Results indicated that this CTE constraint layer could reduce the thermal mismatch between silicon die and substrate, as well as enhance the reliability of the solder joint. The results show that this new flip chip package can achieve the same level of solder joint reliability as the conventional flip chip package using an underfill material. Compared to the conventional flip chip package, results indicate that the reliability life of both the conventional flip chip and the new flip chip package with a 0.1 mm constraint layer both satisfy the life-cycle design specifications. Thus, the CTE constraint layer would be a feasible way to replace the underfill material such that better reworkability of the package can be attained.

REFERENCES

- [1] J. Giesler, S. Machuga, G. O'Malley, and M. Williams, "Reliability of flip chip on board assemblies," in *Proc. 1st Int. Symp. Flip Chip Technol.*, San Jose, CA, Feb. 15–18, 1994, pp. 127–135.
- [2] K. Darbha and J. H. Okura, "Impact of underfill filler particles on reliability of flip-chip interconnects," *IEEE Trans. Comp., Packag., Manuf. Technol. A*, vol. 21, pp. 275–280, June 1998.
- [3] S. Rzepka, M. A. Korhonen, E. Meusel, and C.-Y. Li, "The effect of underfill and underfill delamination on the thermal stress in flip-chip solder joints," *Trans. ASME, J. Electron. Packag.*, vol. 120, pp. 342–348, 1998.

- [4] C. P. Wong and D. F. Baldwin, "Next generation of novel no flow underfills for low-cost flip-chip applications: Materials and processes," *Future Circuits Int.*, pp. 67–70, 1998.
- [5] E. Madenci, S. Shkarayev, and R. Mahajan, "Potential failure sites in a flip-chip package with and without underfill," *Trans. ASME, J. Electron. Packag.*, vol. 120, pp. 336–341, 1998.
- [6] C. P. Yeh, W. X. Zhou, and K. Wyatt, "Parametric finite element analysis of flip chip reliability," *Int. J. Microcirc. Electron. Packag.*, vol. 19, no. 2, pp. 120–127, 1996.
- [7] Y. H. Pao, S. Badgley, R. Govila, L. Baumgarter, R. Allor, and R. Cooper, "Measurements of mechanical behavior of high lead lead-tin solder joints subjected to thermal cycling," *Trans. ASME, J. Electron. Packag.*, vol. 114, pp. 135–145, 1992.
- [8] H. C. Cheng, K. N. Chiang, and C. K. Chen, "Parametric analysis of thermally enhanced BGA reliability using a finite-volume-weighted averaging technique," in *Proc. ASME Winter Annu. Meeting, Thermo-Mech. Characterization Evolving Packag. Mater. Structures Symp.*, vol. EEP-24, Anaheim, CA, Nov. 15–20, 1998, pp. 13–20.
- [9] K. N. Chiang, H. C. Cheng, and W. H. Chen, "Large-scaled 3-D area array electronic packaging analysis," *J. Comput. Modeling Simulation Eng.*, vol. 4, no. 1, pp. 4–11, 1999.
- [10] H. C. Cheng, K. N. Chiang, and M. H. Lee, "An alternative local/global finite element approach for ball grid array typed packages," *ASME Trans., J. Electron. Packag.*, vol. 120, pp. 129–134, 1998.
- [11] K. N. Chiang and W. L. Chen, "Electronic packaging reflow shape prediction for the solder mask defined ball grid array," *ASME Trans., J. Electron. Packag.*, vol. 120, pp. 175–178, 1998.
- [12] K. N. Chiang, Y. T. Lin, and H. C. Cheng, "On enhancing eutectic solder joint reliability using a second-reflow-process approach," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 9–14, Feb. 2000.
- [13] L. F. Coffin, Jr. and N. Y. Schenectady, "A study of the effects of cyclic thermal stresses on a ductile metal," *ASME Trans.*, vol. 76, pp. 931–950, 1954.
- [14] S. S. Manson, "Mechanics," *Exper. Mech.*, vol. 5, no. 7, pp. 193–226, 1965.

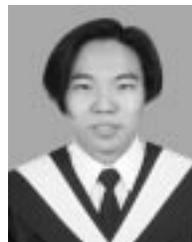


Kuo-Ning Chiang received the Ph.D. degree from the Georgia Institute of Technology, Atlanta, in 1989.

He has more than 13 years of industrial/research experience in analysis, design, and development of electromechanical systems and CAE applications. Between 1989 and 1993, he was a Senior Engineer with the R&D Division, MacNeal-Schwendler Corporation. In 1993, he joined the National Center for High-Performance Computing (NCHC), Taiwan, R.O.C., as Division Head of R&D Division I. In August 1998, he became Associate Professor of power mechanical engineering, National Tsing Hua University, Taiwan. He has published more than 70 conference/journal papers in the area of CAE and electronic packaging. He was responsible for more than ten electronic packaging projects that related to the solder reflow, package simulation/design, and reliability analysis of electronic devices. Currently, he hold three U.S. and five Taiwan Electronic Packaging Device patents, and he has five U.S. and 12 Taiwan Electronic Packaging/Optical Device patents pending.

Zheng-Nan Liu is pursuing the M.S. degree in power mechanical engineering at the National Tsing Hua University, Taiwan, R.O.C.

He is a Graduate Assistant in the Power Mechanical Engineering Department, National Tsing Hua University.



Chih-Tang Peng is pursuing the M.S. degree in power mechanical engineering at the National Tsing Hua University, Taiwan, R.O.C.

He is a Graduate Assistant in the Power Mechanical Engineering Department, National Tsing Hua University.